

QIQY5


Whisky3.0 (Y400S)

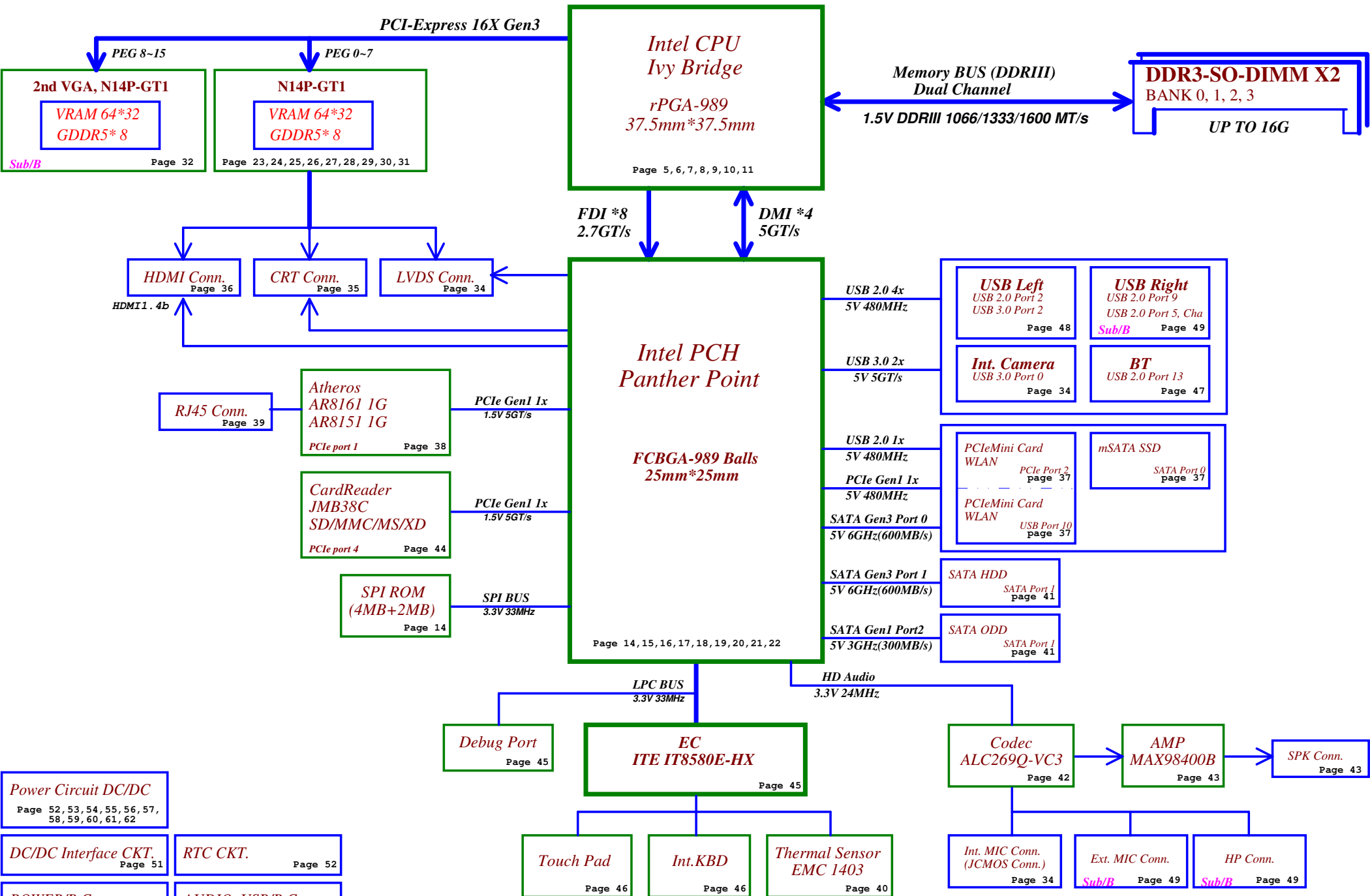
NM-A141 Rev0.2 Schematic

***Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N14P GT + 2nd VGA N14P GT***

2012-10-25-Rev0.2

Security Classification	LC Future Center Secret Data			Title	
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
	XHCI	1	Camera
		2	
		3	USB Port (Left Side)
		4	
		5	USB Port (Right Side)
		6	
		7	
		8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR815168161 LAN surge part --> Delete (201200627)
61@	X76 P/N for AR8161
51@	X76 P/N for AR8151
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
OPT@	For optimum function part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module
EC_SMB_CK1	IT8580E			V	X	X	X	X	X	X
EC_SMB_DA1	+3VALW	X	X	+3VALW	X	X	X	X	X	X
EC_SMB_CK2	IT8580E	V	V	X	X	X	X	V	V	X
EC_SMB_DA2	+3VS	+3VS	+3VS					+3VS	+3V_PCH	
SMB_CLK_S3	PCH	X	X	X	X	V	V	X	V	V
SMB_DATA_S3	+3VS					+3VS	+3VS		+3V_PCH	+3VS

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb



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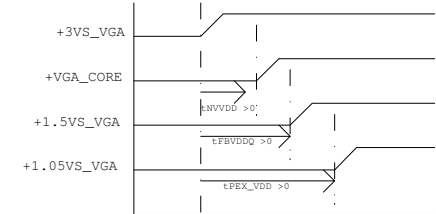
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NOTES LIST	Y400S-NM-A141	1.0
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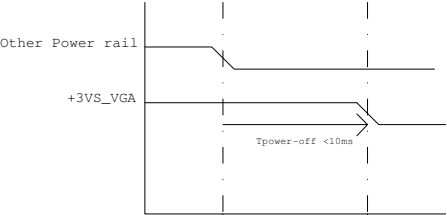
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB_CLAMP
GPIO1	OUT	-	
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	
GPIO6	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO7	OUT	-	
GPIO8	I/O	-	OVERT#
GPIO9	OUT	-	VGA_ALERT#
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	NVVD PWM_VID
GPIO12	IN		VGA_AC_DET_R (10K pull High)
GPIO13	OUT	-	DPRS LPVR_VGA
GPIO14	OUT	-	
GPIO15	IN	N/A	
GPIO16	OUT	-	
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Device ID		setting		I2C Slave addresses ID	
N13P-GT (28nm)	0x0FDB	SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E	
			1	0x9C	

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

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Title

VGA NOTES LIST

Size Custom

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Y400S-NM-A141

Rev

1.0

Date

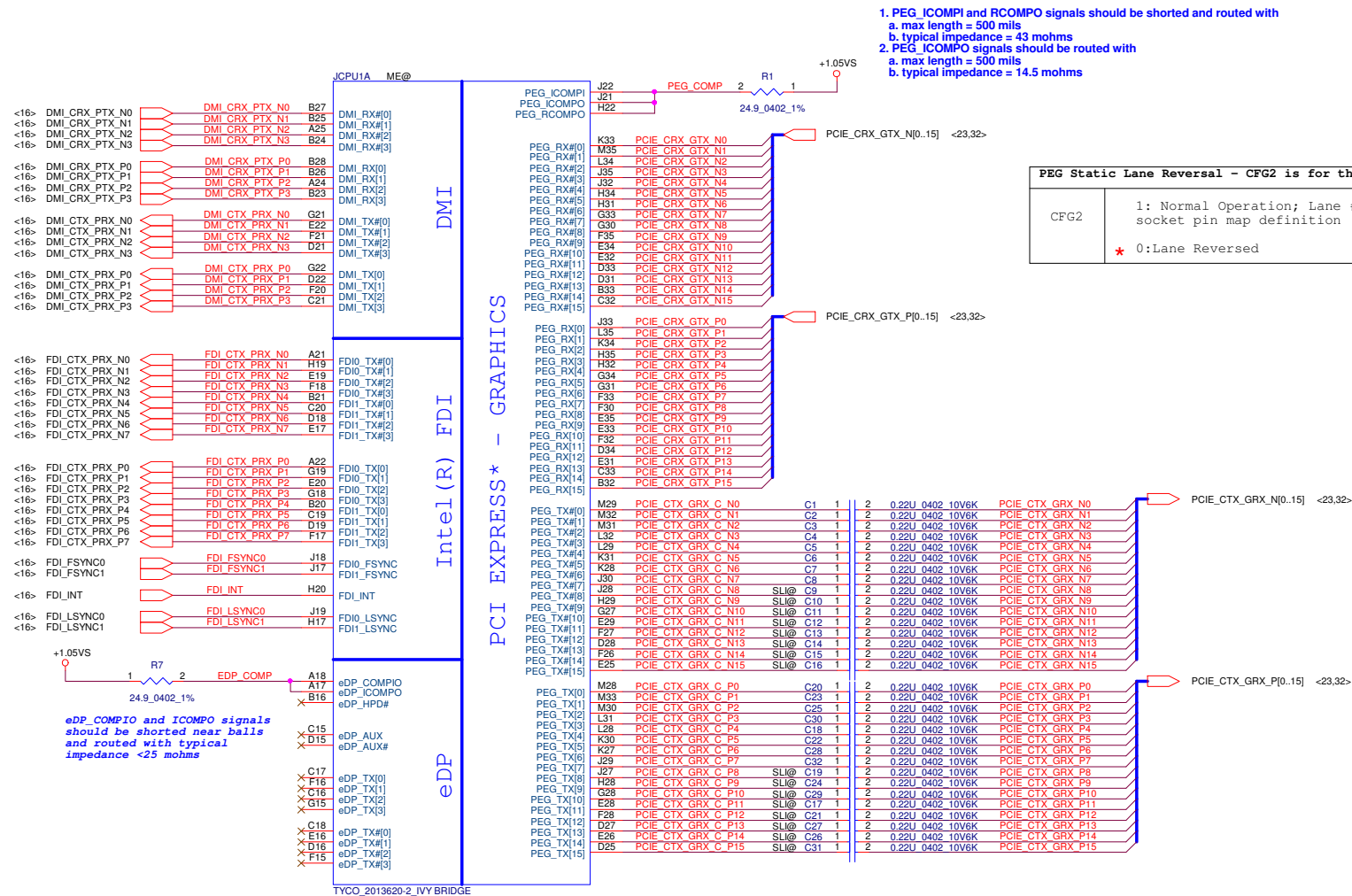
Monday, January 14, 2013

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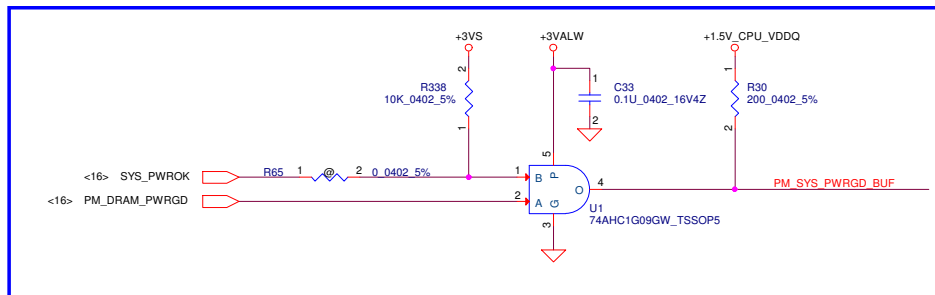
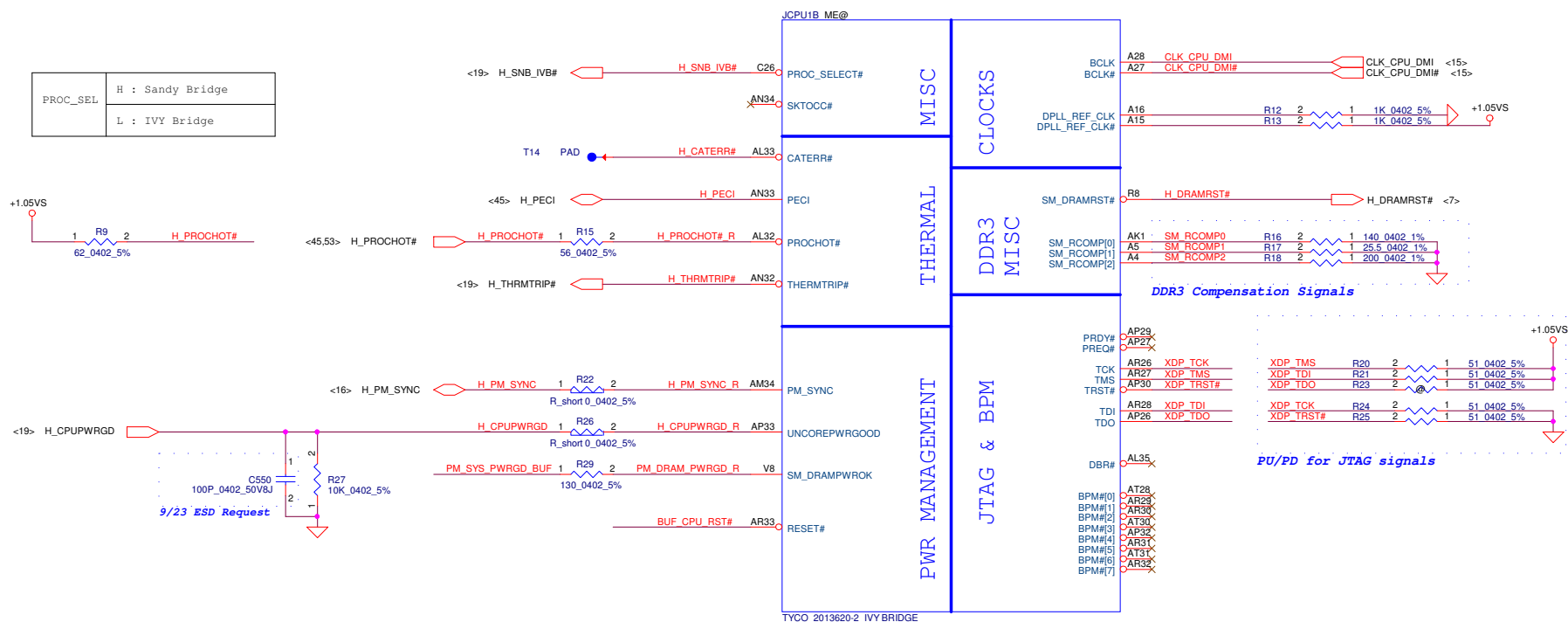
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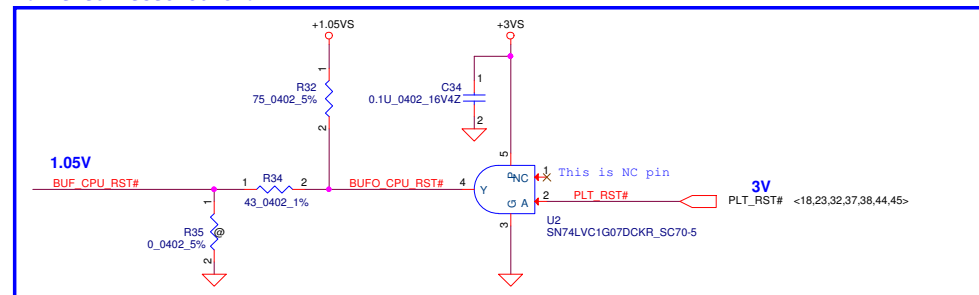
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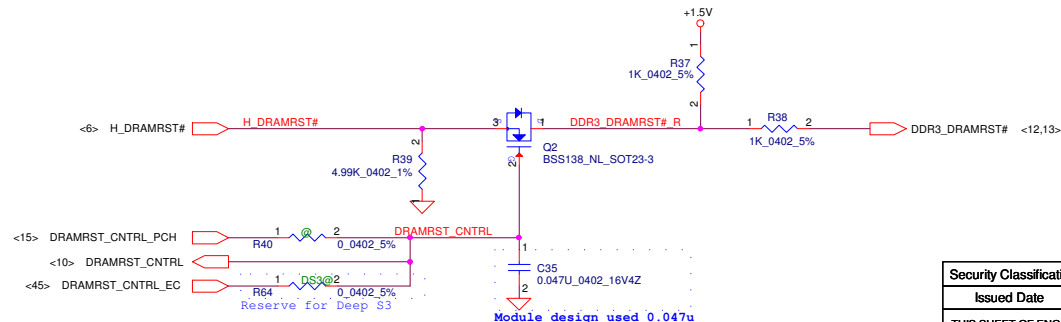
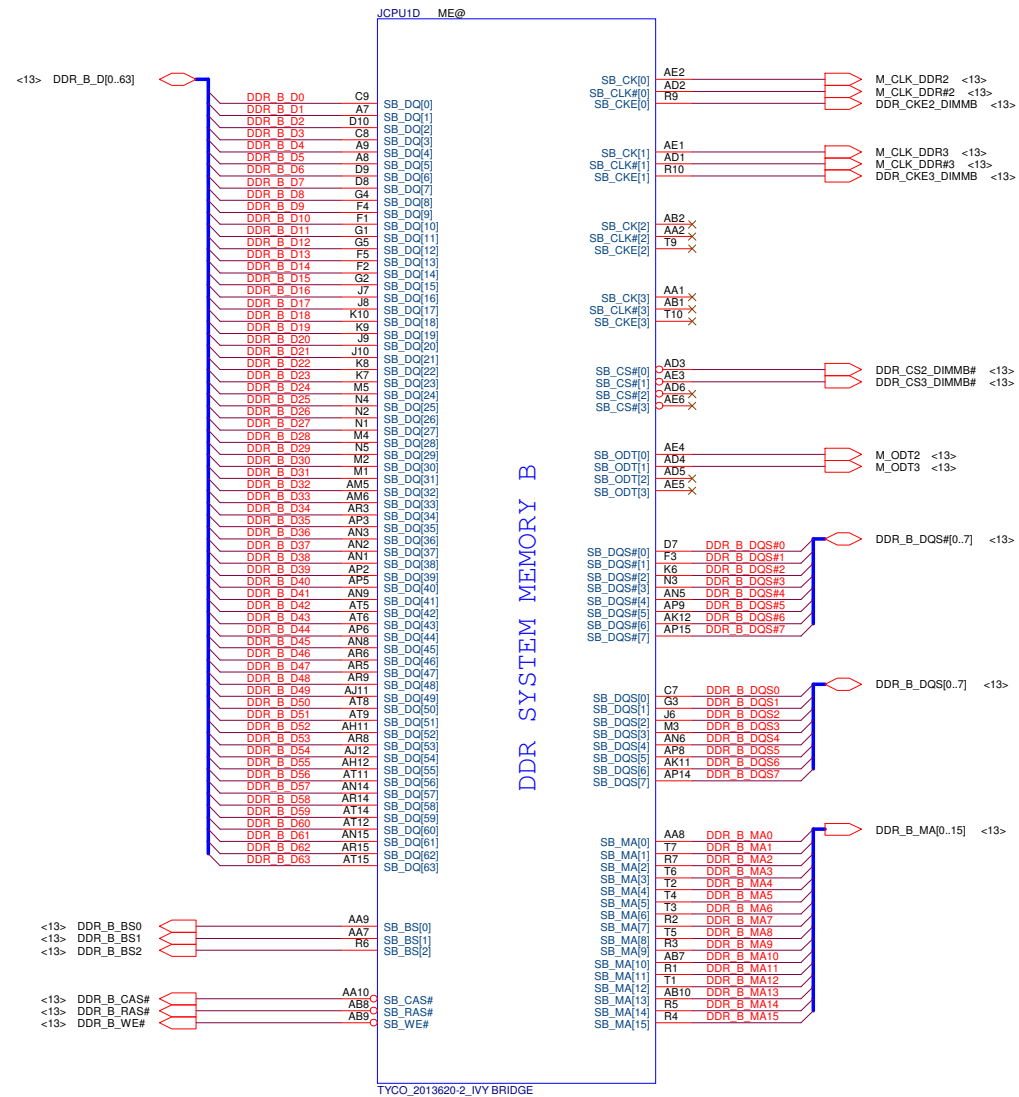
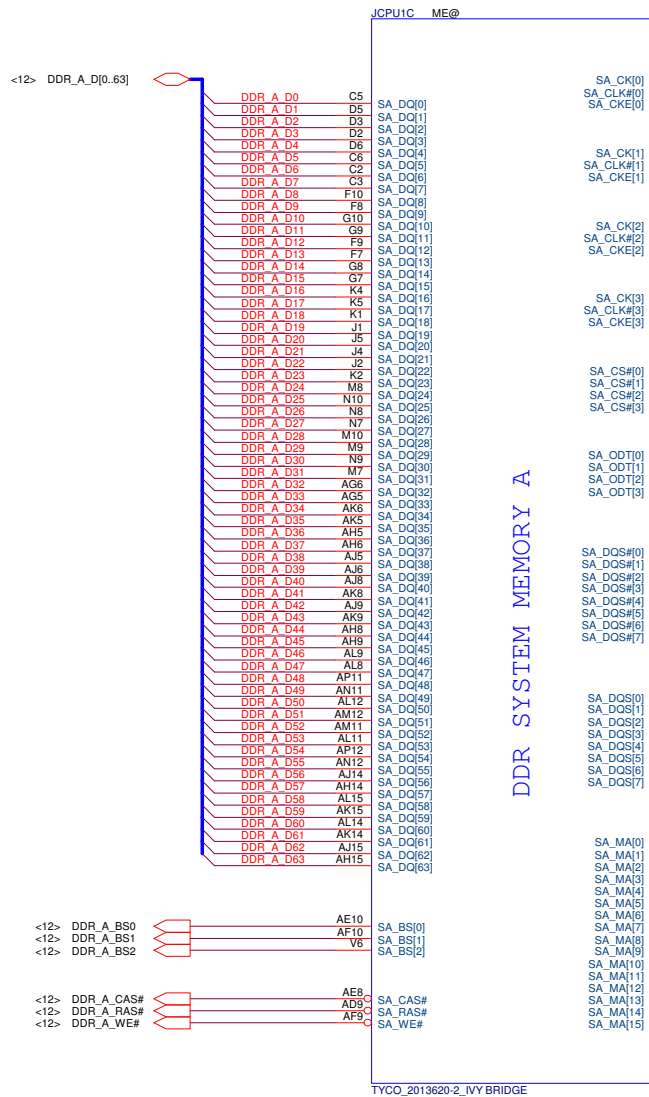



PROC_SEL	H : Sandy Bridge
	L : IVY Bridge

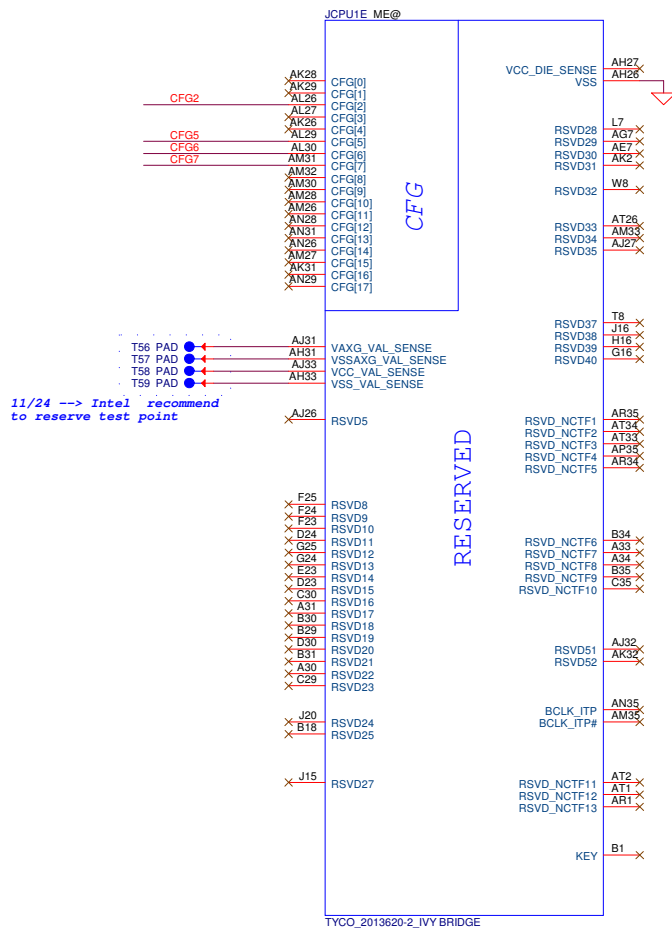


Buffered Reset to CPU

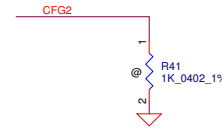




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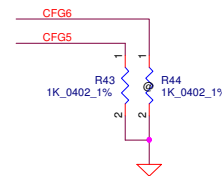


CFG Straps for Processor

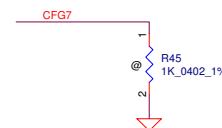


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<p>★ 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>

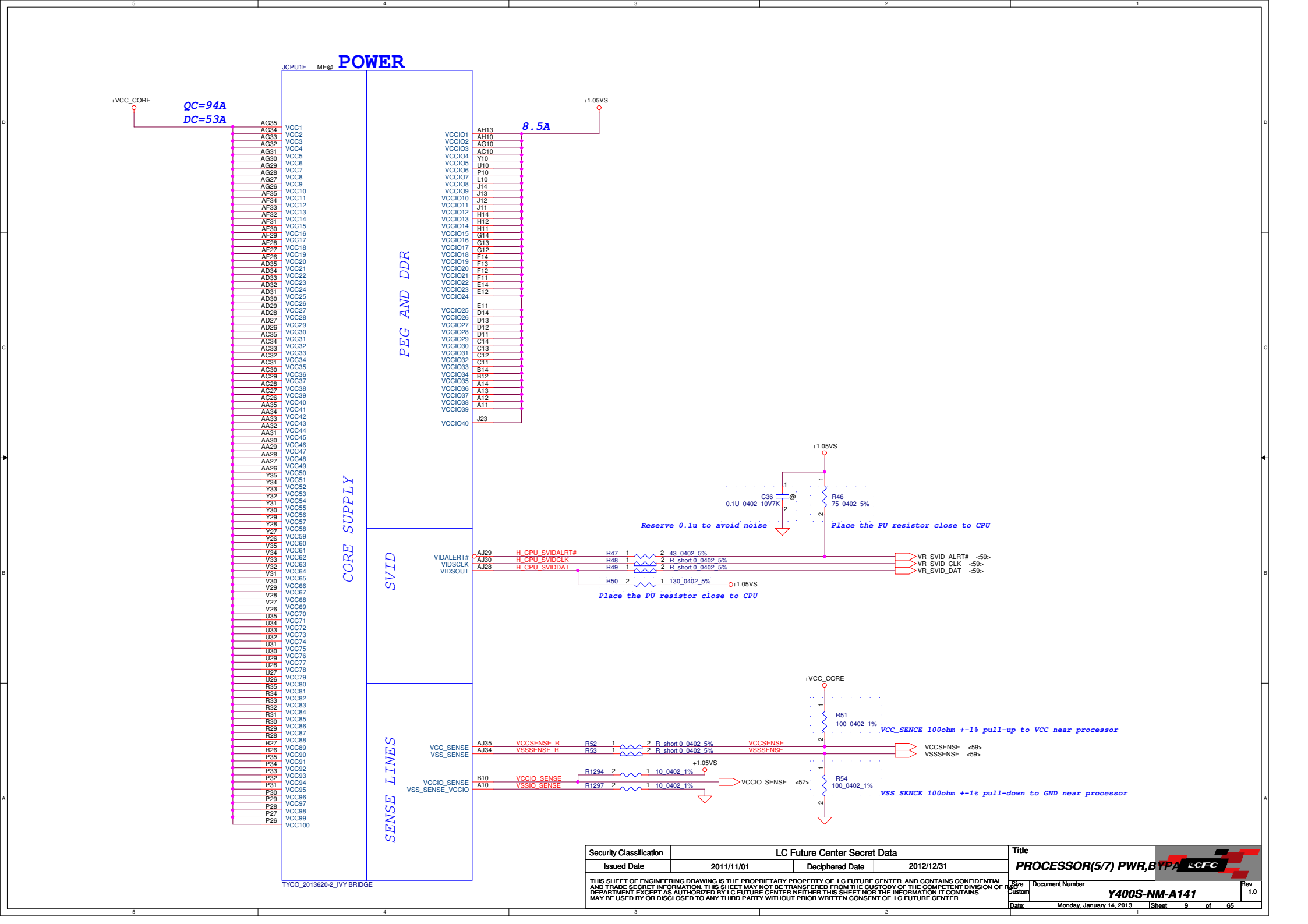
Display Port Presence Strap	
CFG4	<p>★ 1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>



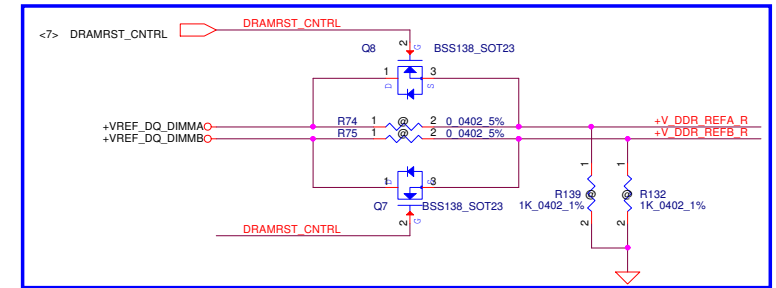
PCIe Port Bifurcation Straps	
CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>★ 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>



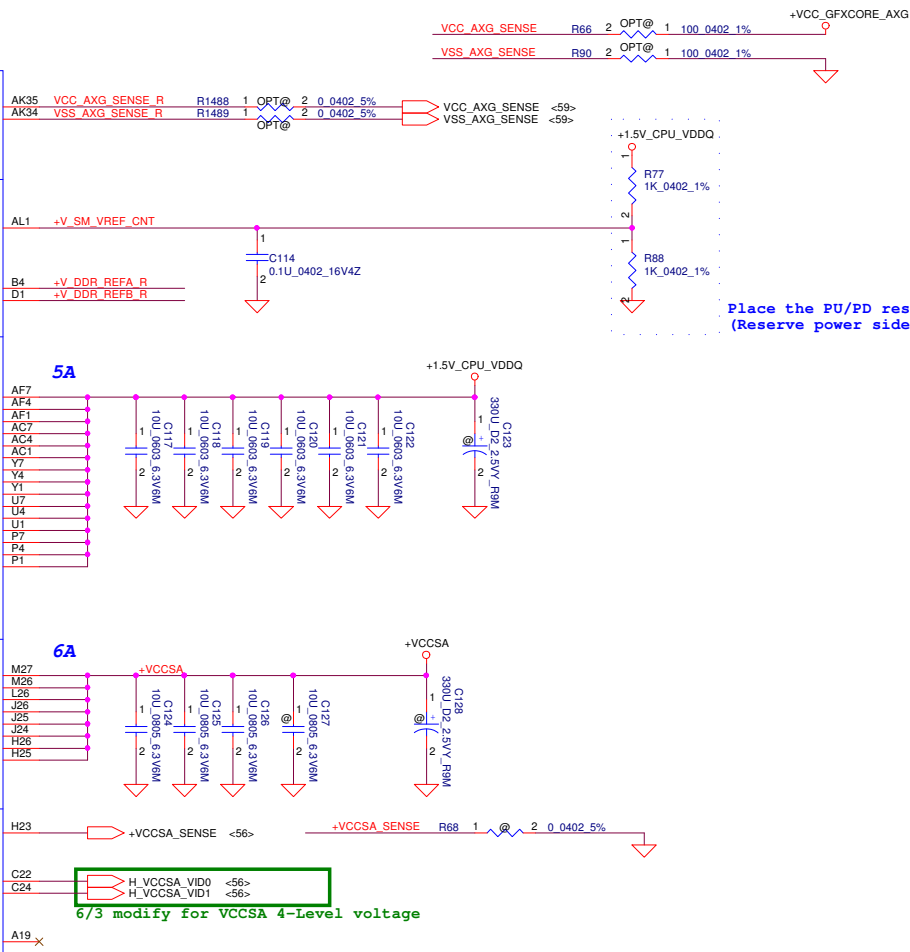
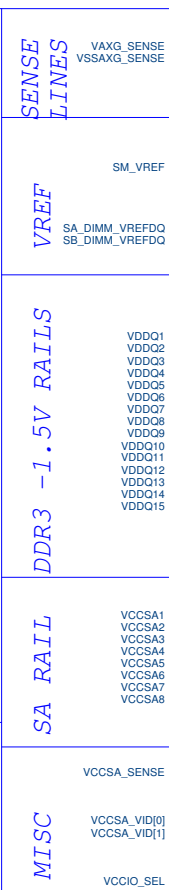
PEG DEFER TRAINING	
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>



For Deep S3




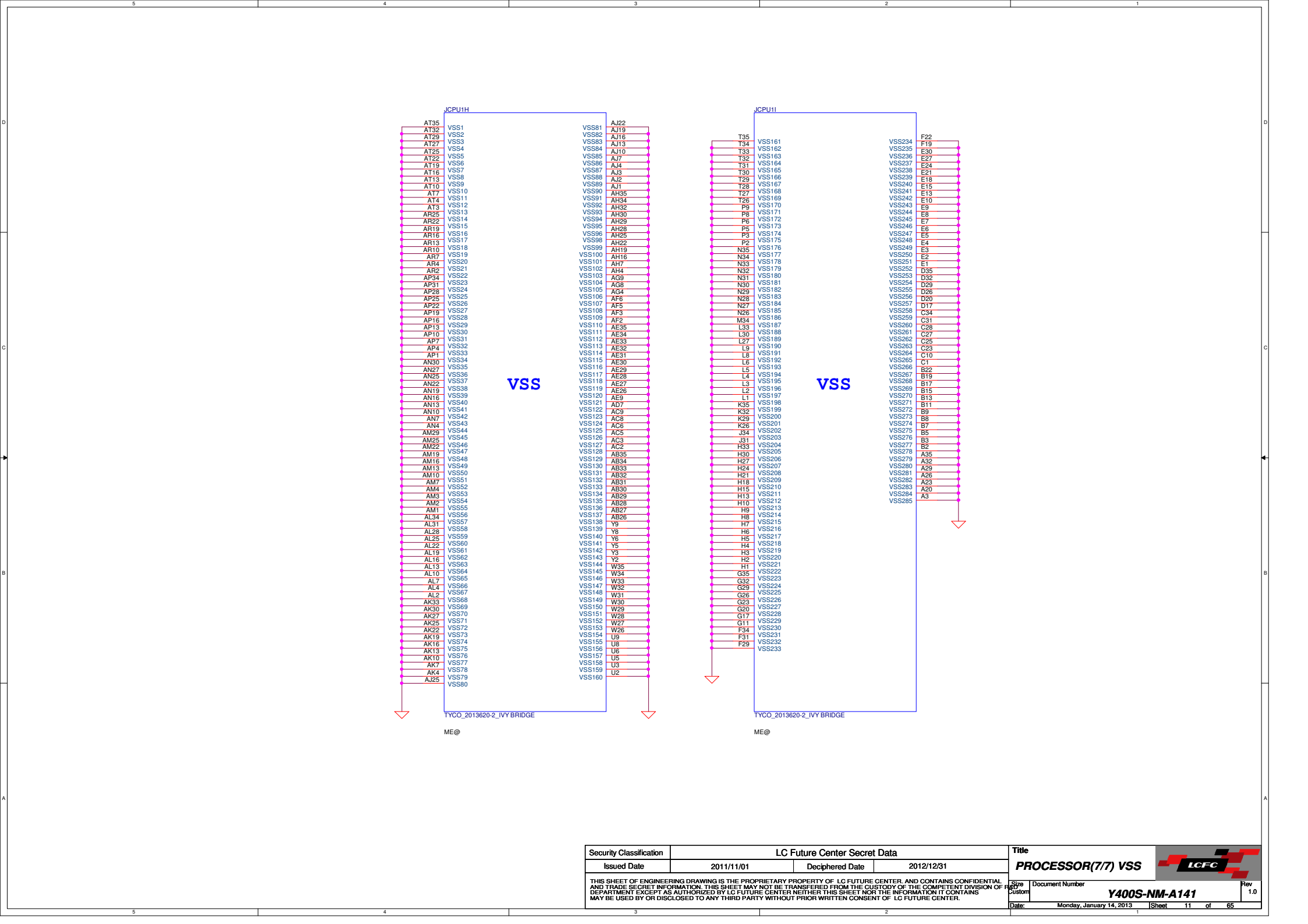
POWER

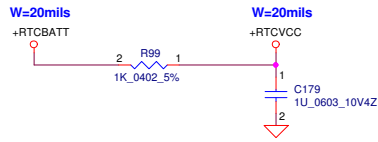


6/3 modify for VCCSA 4-Level voltage

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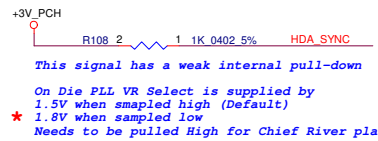
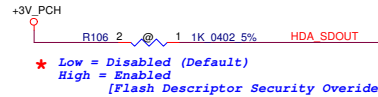
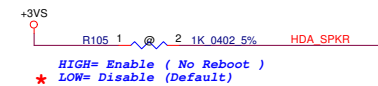
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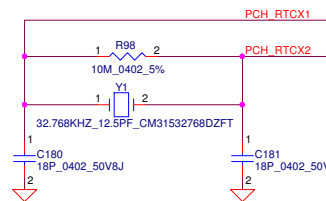
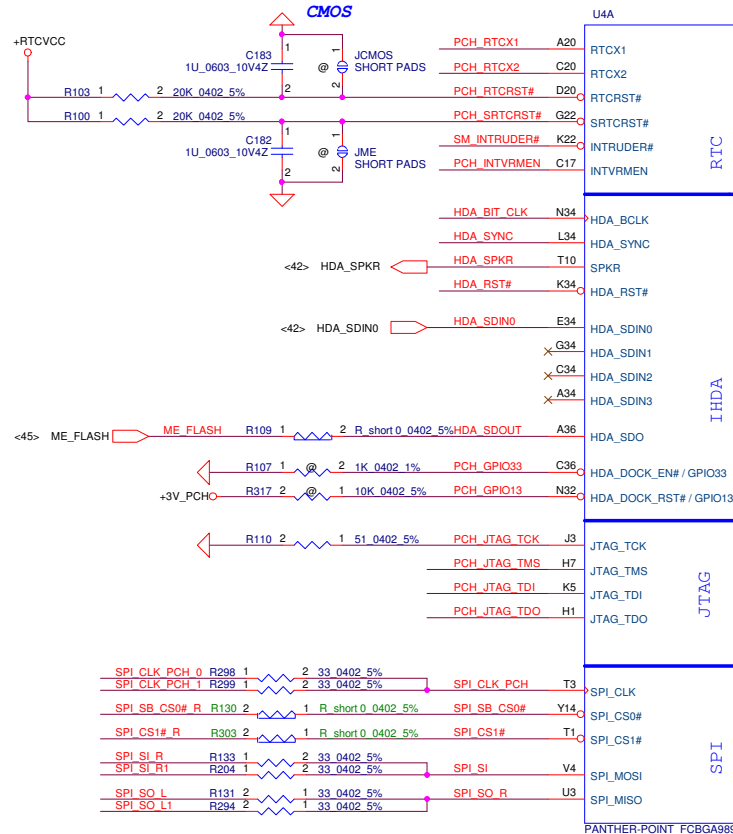
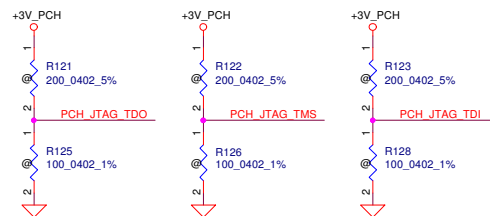
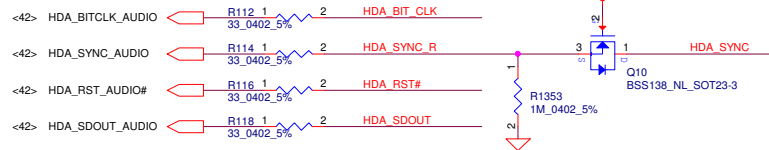


INTVRMEN

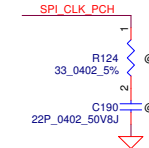
★ H : Integrated VRM enable (Default)
L : Integrated VRM disable
(INTVRMEN should always be pull high.)



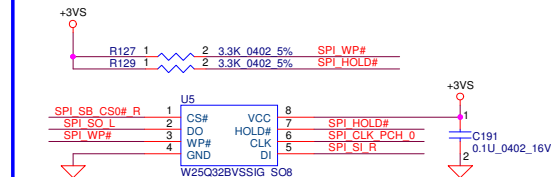
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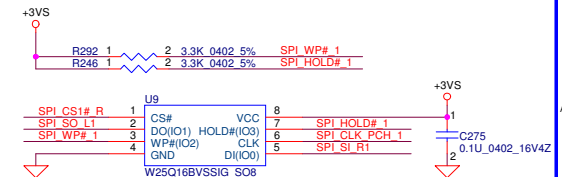
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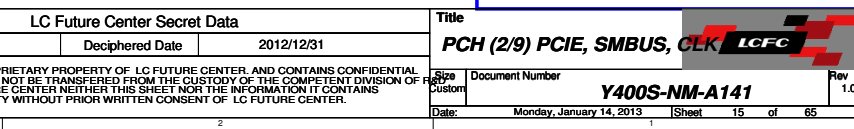
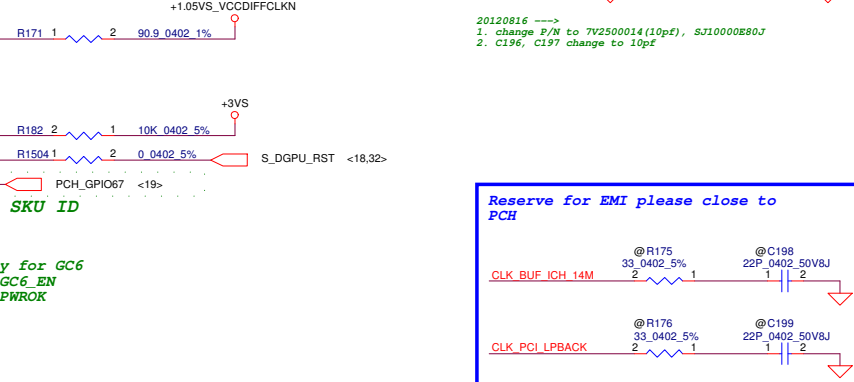
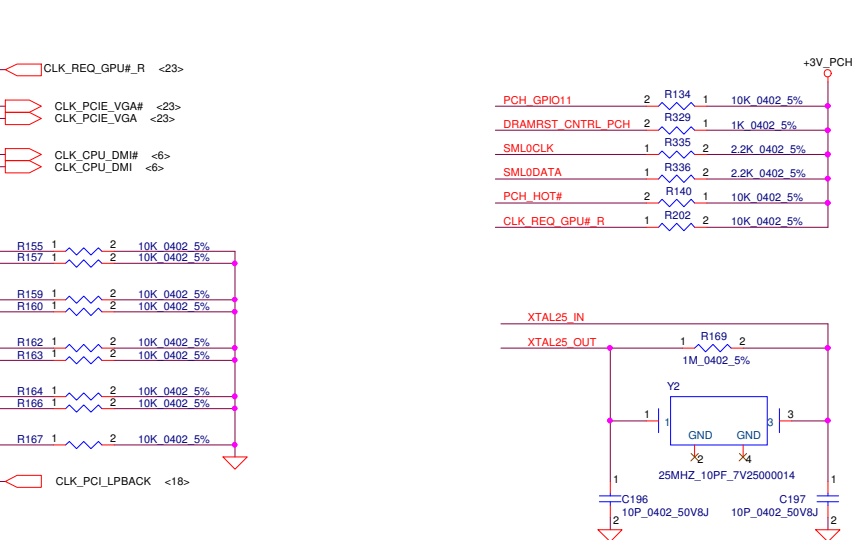
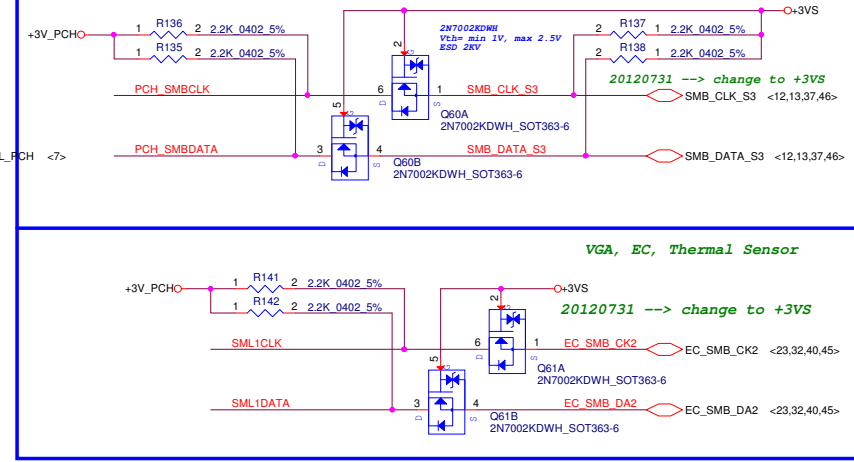
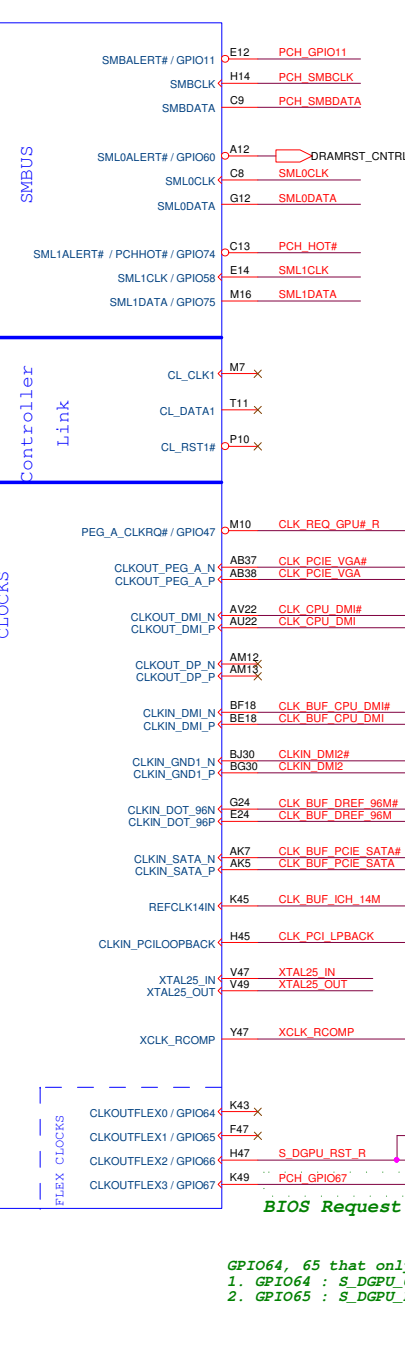
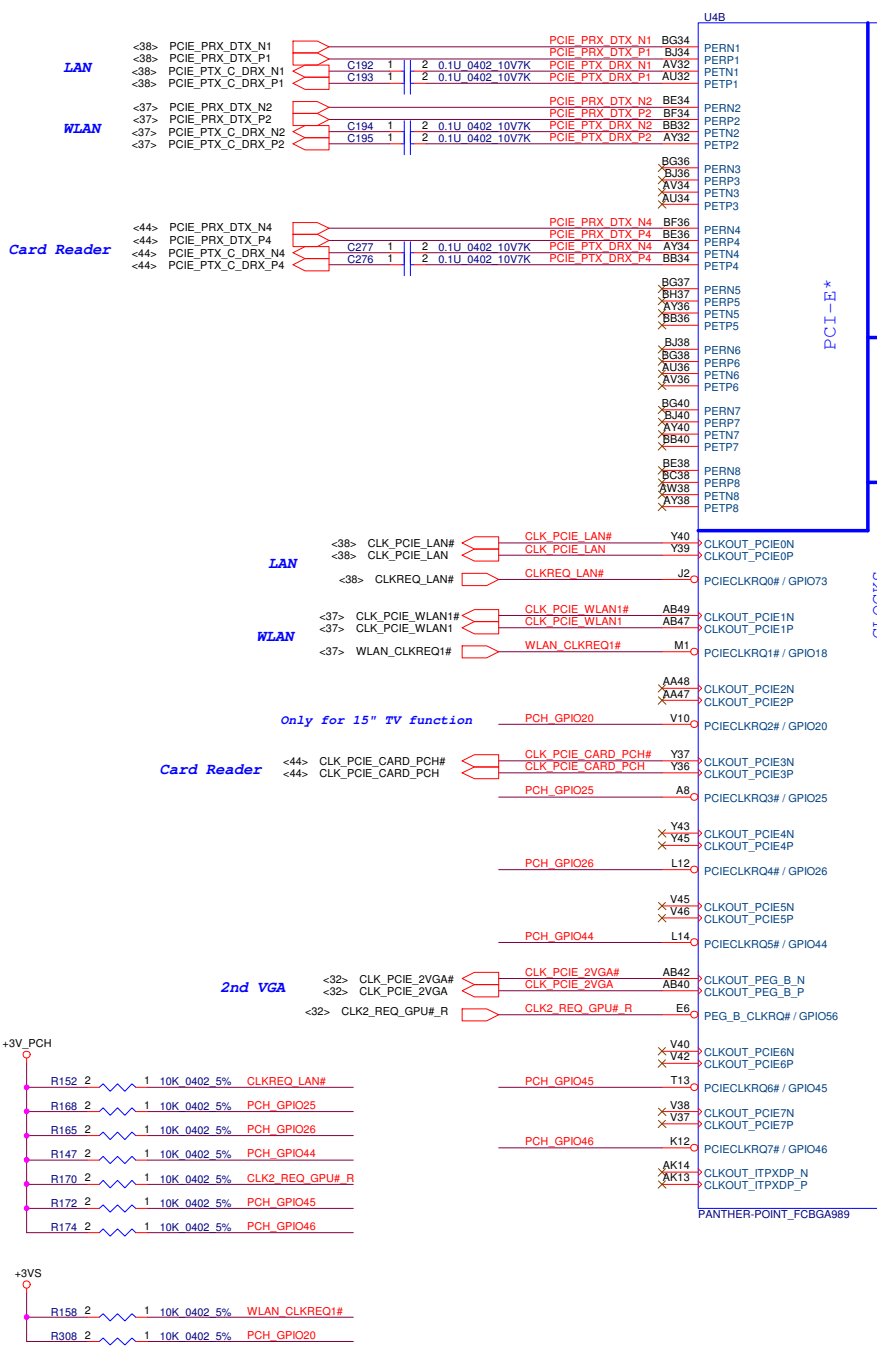
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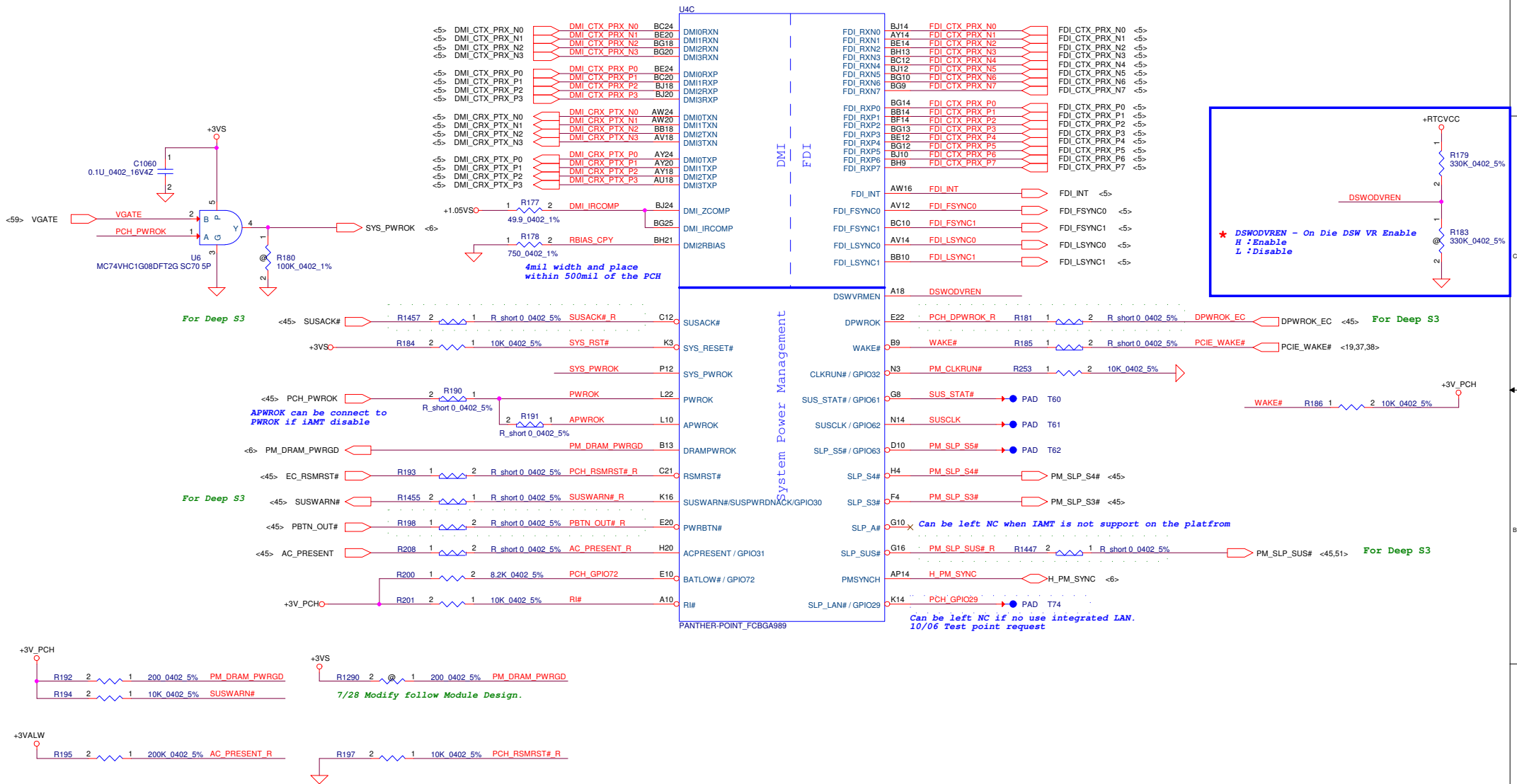
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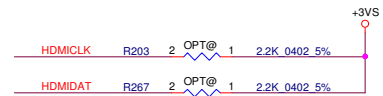
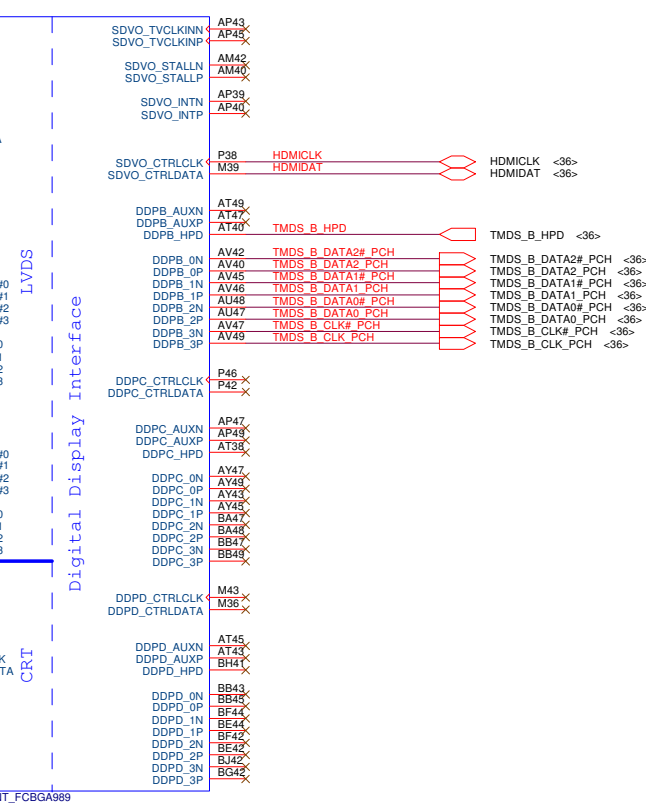
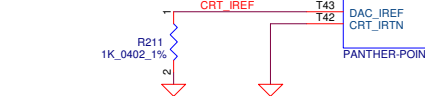
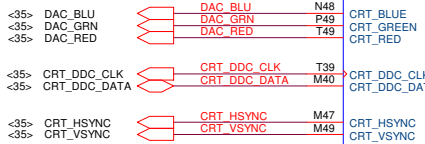
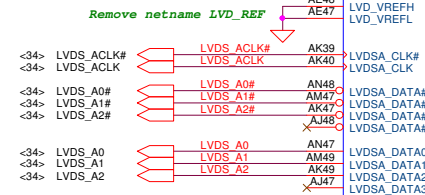
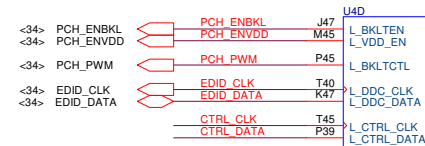
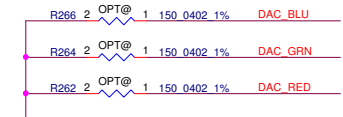
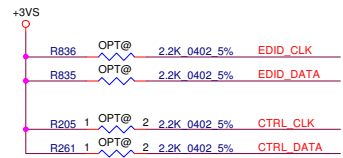


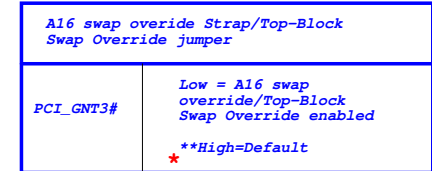
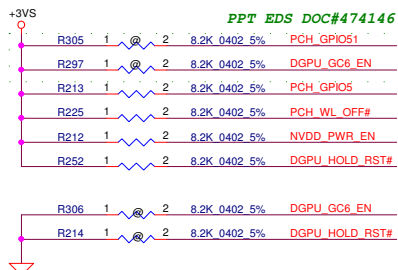
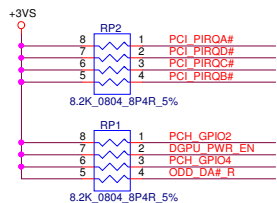
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	PCH (1/9) SATA,HDA,SPI, LPC
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Size	Custom	Document Number	Y400S-NM-A141	
Date:	Monday, January 14, 2013	Sheet	14	of 65
Rev	1.0			



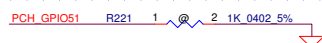
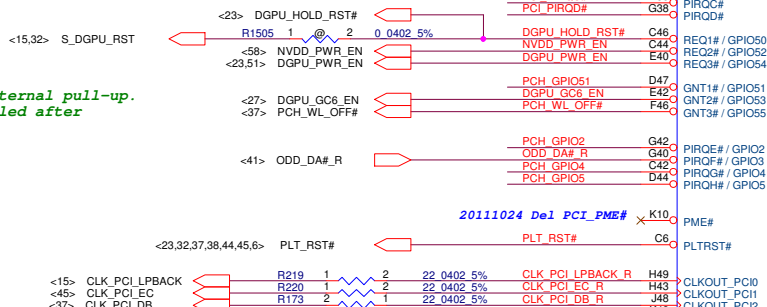
Security Classification	LC Future Center Secret Data		Title	PCH (2/9) PCIE, SMBUS, CLK	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	Size	Document Number
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				Date:	Monday, January 14, 2013
				Sheet	15 of 65
				Rev	1.0



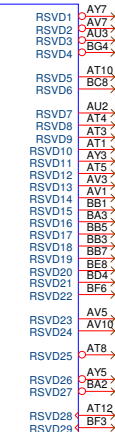
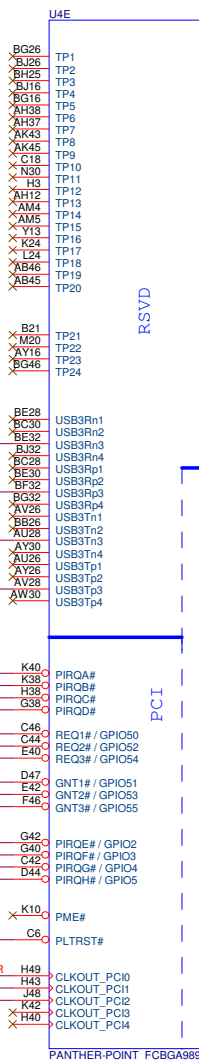
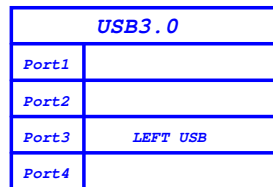




GPI053 => This Signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.



Boot BIOS Strap bit1 BBS1		
	Bit11	Bit10
GNT1#/ GPI051	0	1
	1	0
	1	1
	0	0
		Destination
		Reserved
		Reserved
		★ SPI (Default)
		LPC



USB DEBUG = PORT1 AND PORT9

Camera

LEFT USB

RIGHT USB 1 (CHARGER PORT, SUB/B)

Some PCH config not support USB port 6 & 7.

RIGHT USB 2 (SUB/B)

WLAN

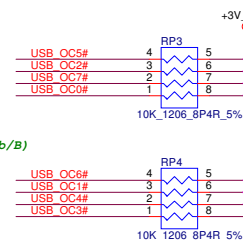
BT

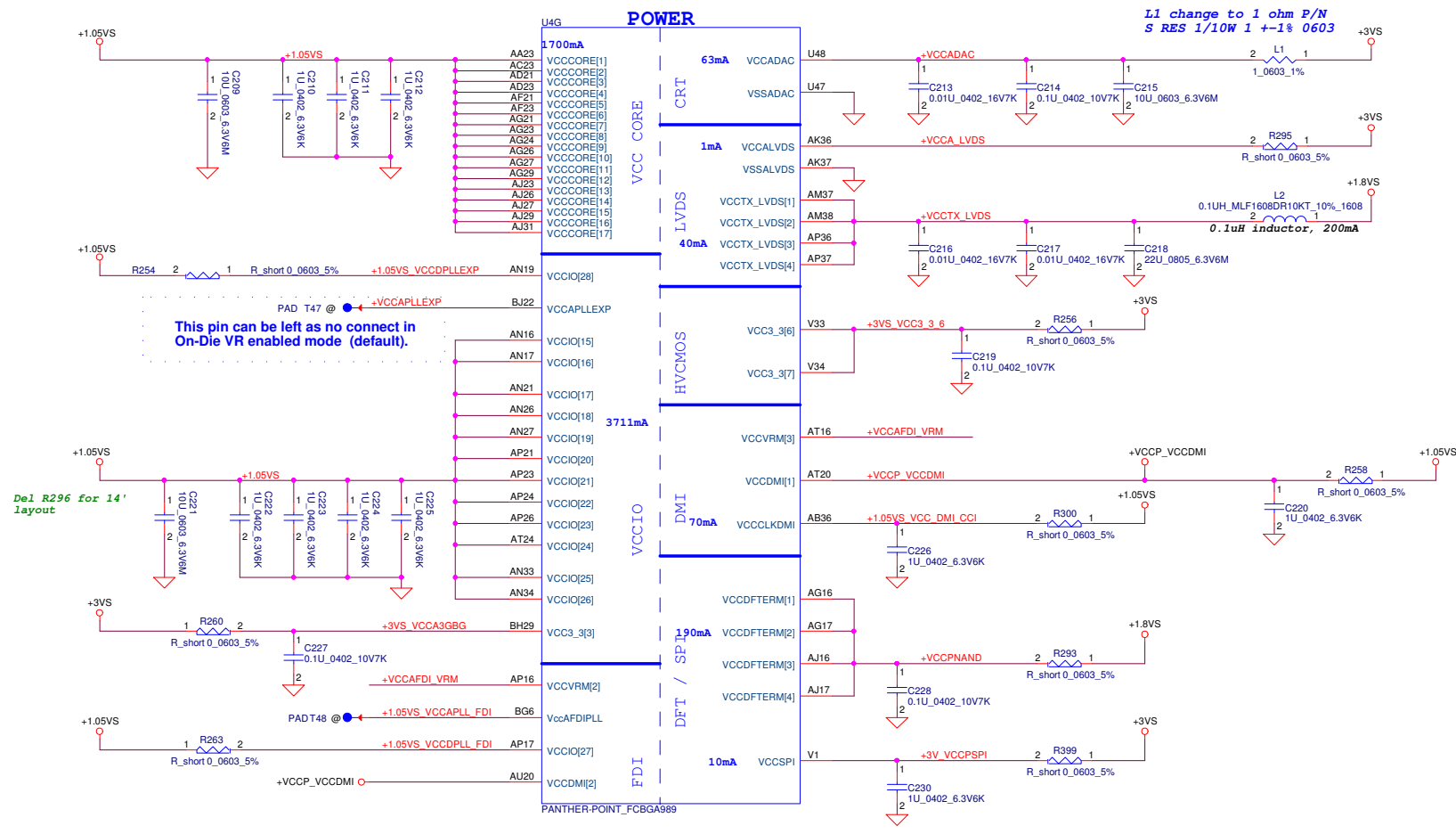
Within 500 mils

USB3 Port3, USB2 Port2

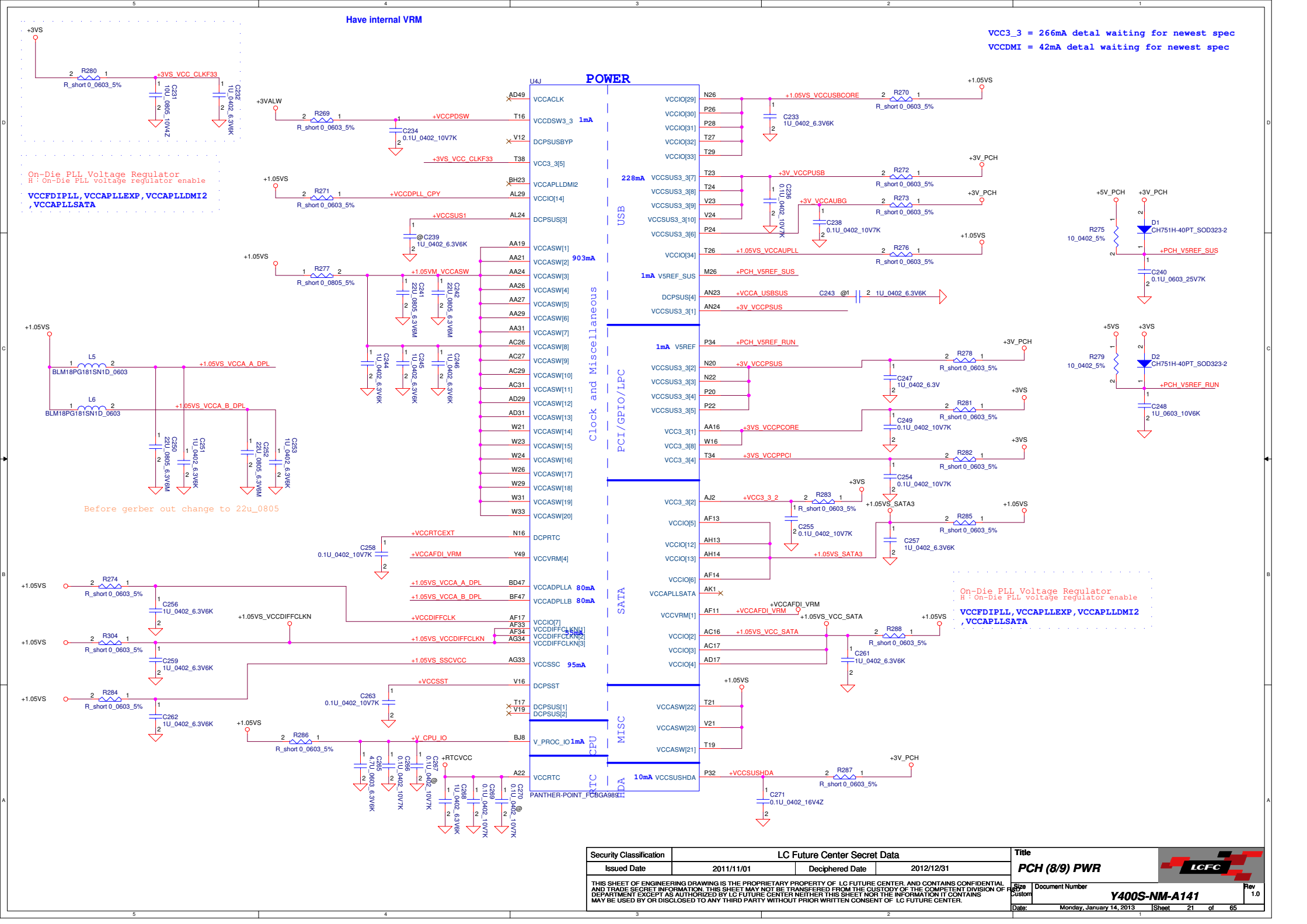
USB2 Port5, Charger Port

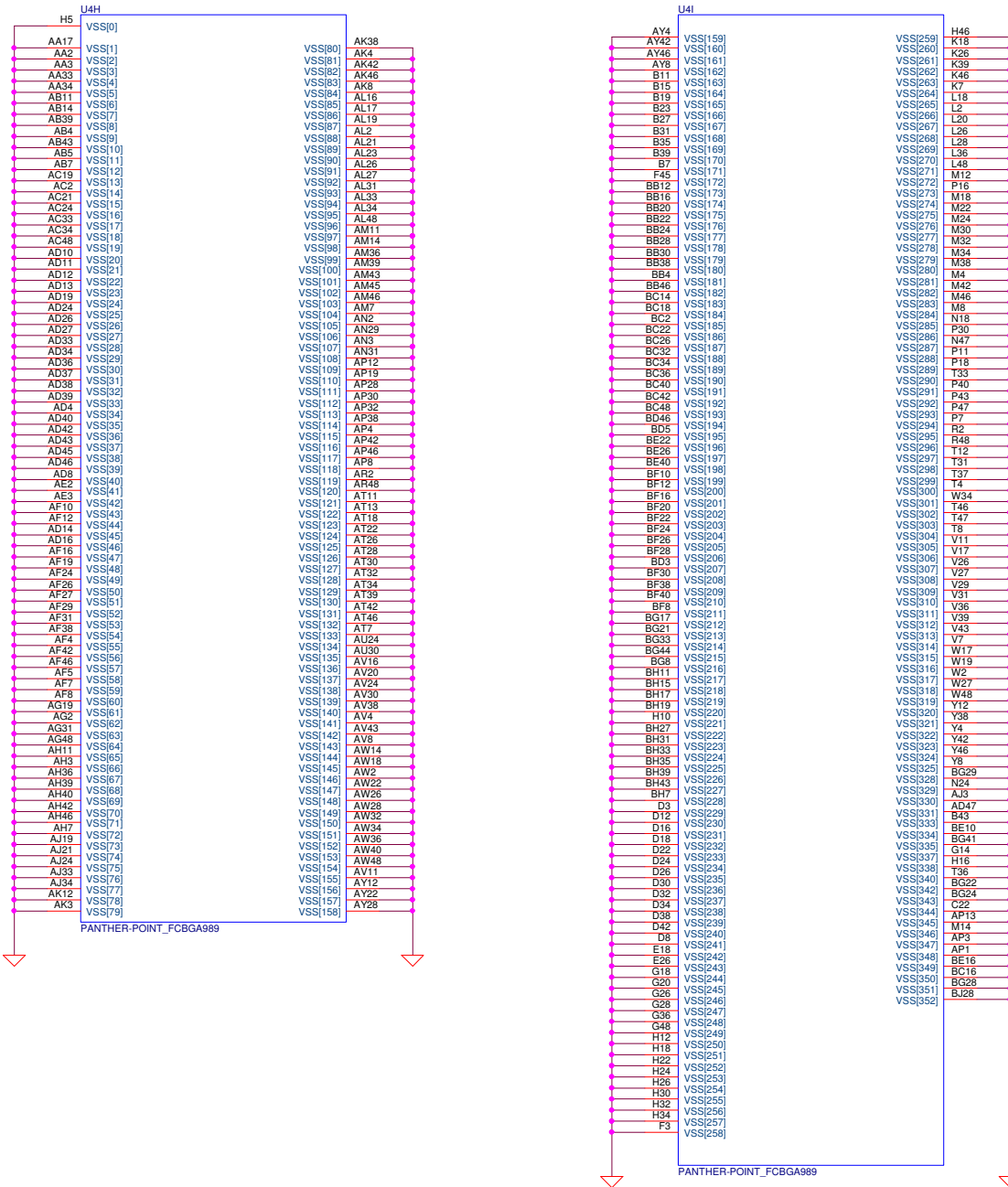
USB2 Port9, Right USB (Sub/B)



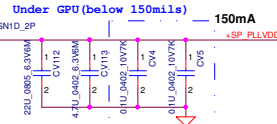


PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

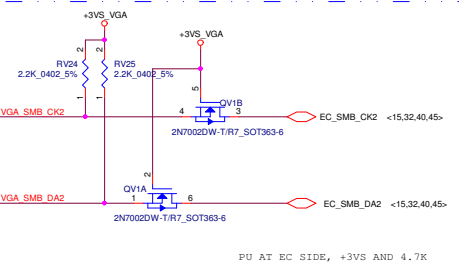




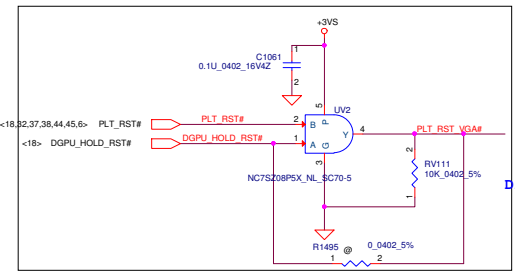
<32.5> PCIE_CTX_GRX_N0.15]
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 <32.5> PCIE_CTX_GTX_N0.15]
 <32.5> PCIE_CTX_GTX_P0.15]



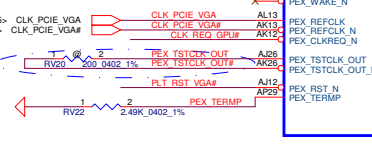
180ohms (ESR=0.2) Bead



PCIE_CRX_GTX_P7	CV24	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_P7	AK14	PEX_TX0
PCIE_CRX_GTX_N7	CV25	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_N7	AK14	PEX_TX0_N
PCIE_CRX_GTX_P6	CV21	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_P6	AK14	PEX_TX1
PCIE_CRX_GTX_N6	CV23	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_N6	AK14	PEX_TX1_N
PCIE_CRX_GTX_P5	CV25	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_P5	AK15	PEX_TX2
PCIE_CRX_GTX_N5	CV27	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_N5	AK15	PEX_TX2_N
PCIE_CRX_GTX_P4	CV29	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_P4	AK16	PEX_TX3
PCIE_CRX_GTX_N4	CV31	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_N4	AK16	PEX_TX3_N
PCIE_CRX_GTX_P3	CV33	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_P3	AK17	PEX_TX4
PCIE_CRX_GTX_N3	CV35	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_N3	AK17	PEX_TX4_N
PCIE_CRX_GTX_P2	CV30	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_P2	AK17	PEX_TX5
PCIE_CRX_GTX_N2	CV32	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_N2	AK17	PEX_TX5_N
PCIE_CRX_GTX_P1	CV36	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_P1	AK18	PEX_TX6
PCIE_CRX_GTX_N1	CV41	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_N1	AK18	PEX_TX6_N
PCIE_CRX_GTX_P0	CV34	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_P0	AK19	PEX_TX7
PCIE_CRX_GTX_N0	CV35	1	2	0.22U	0.402	10V9K	PCIE_CRX_GTX_N0	AK19	PEX_TX7_N



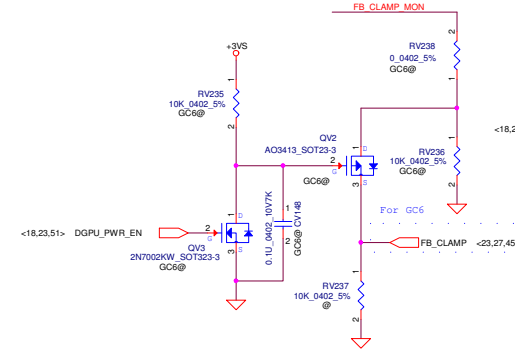
Differential signal



N14P_FCBGA508

GT@

Internal Thermal Sensor



<18.23,51> DGPU_PWR_EN

<15> CLK_REQ_GPU#

<15> CLK_PCIE_VGA#

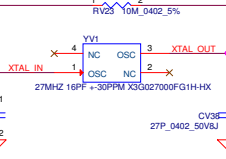
<15> CLK_PCIE_GTX#

<15> CLK_PCIE_VGA#

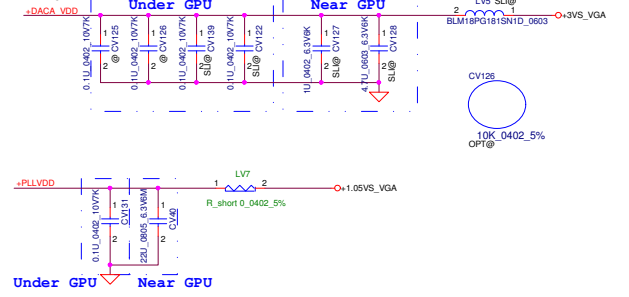
<15> CLK_PCIE_GTX#

<15> CLK_PCIE_VGA#

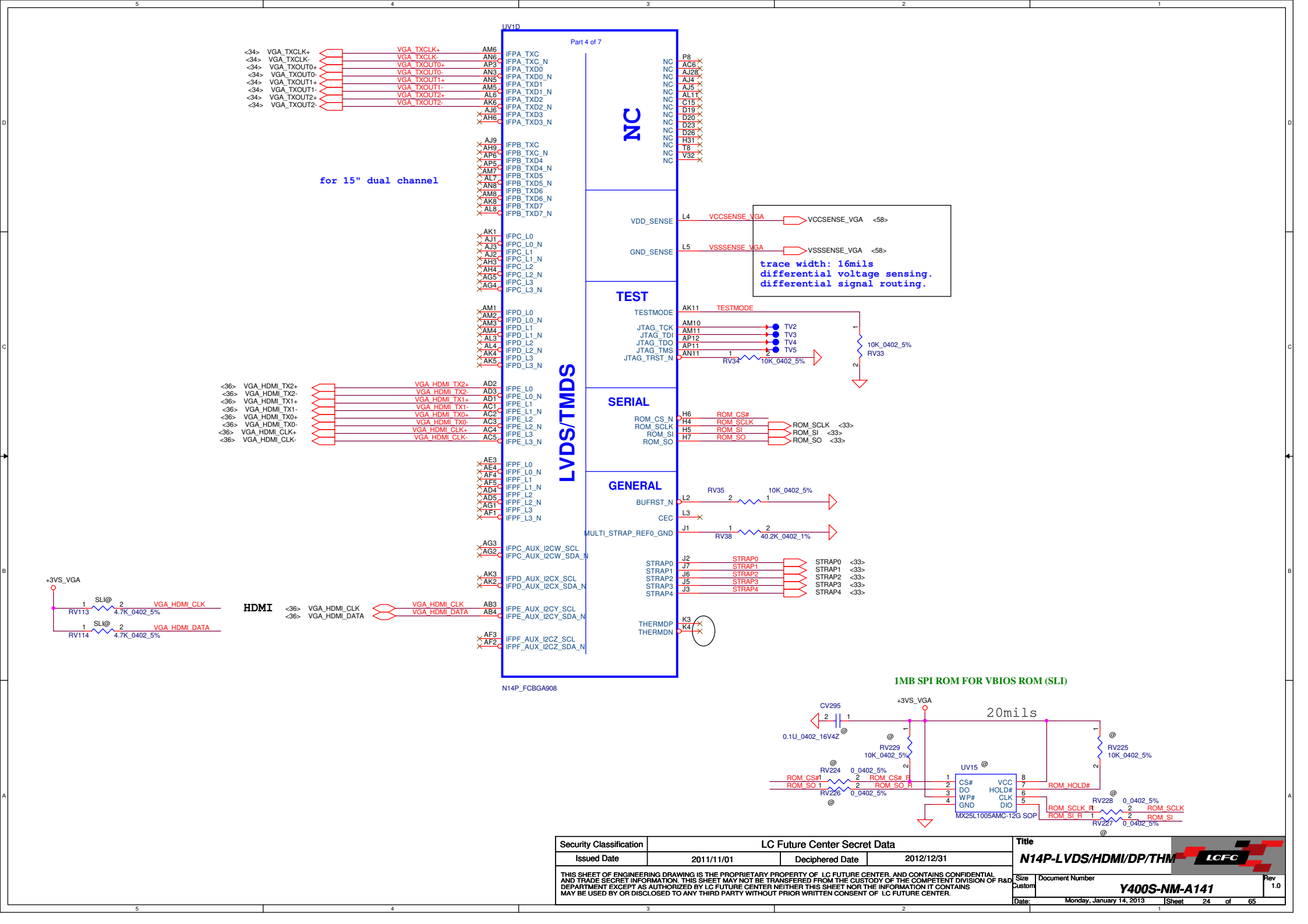
<15> CLK_PCIE_GTX#

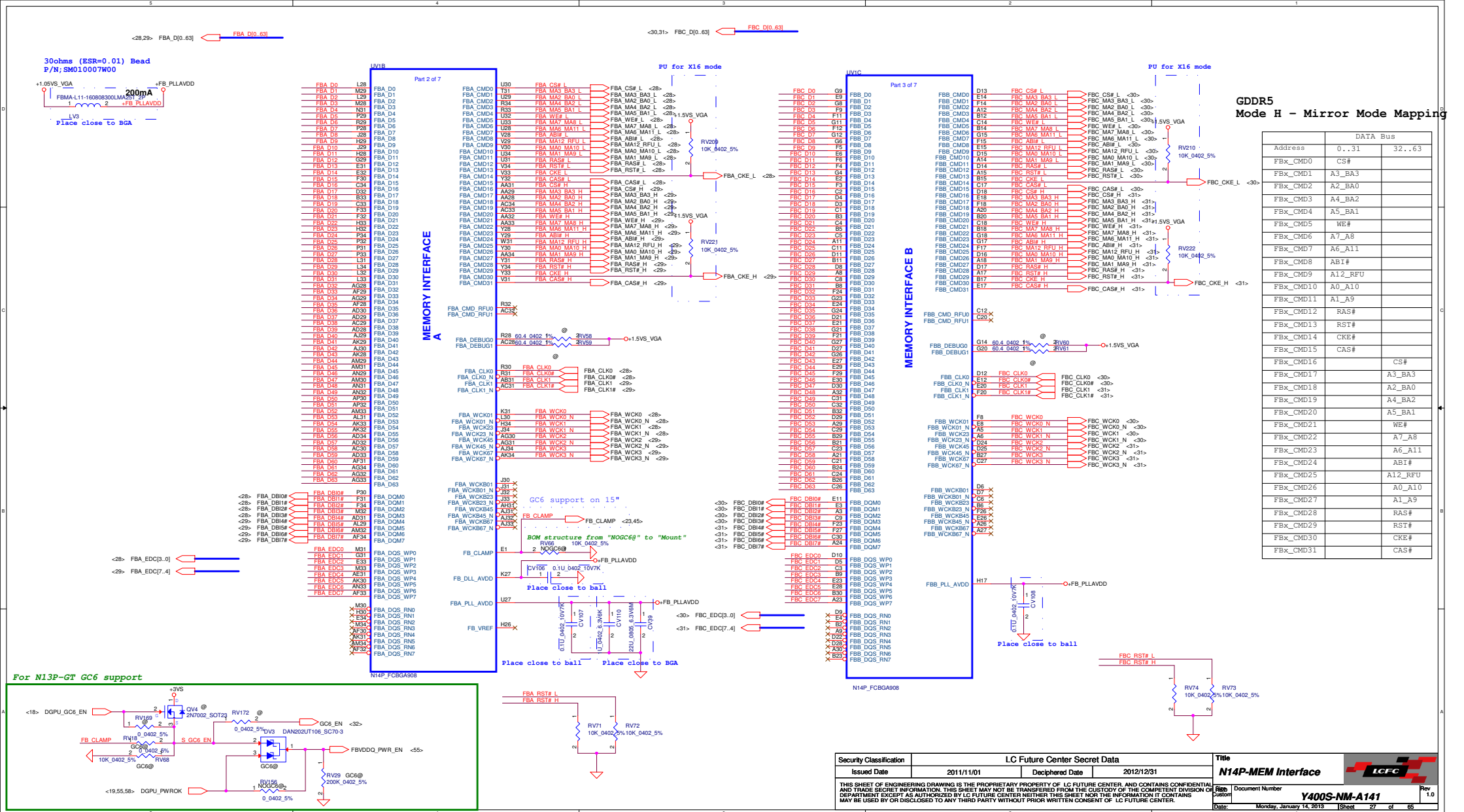


120mA Under GPU Near GPU 220 ohms @100MHz (ESR=0.05)

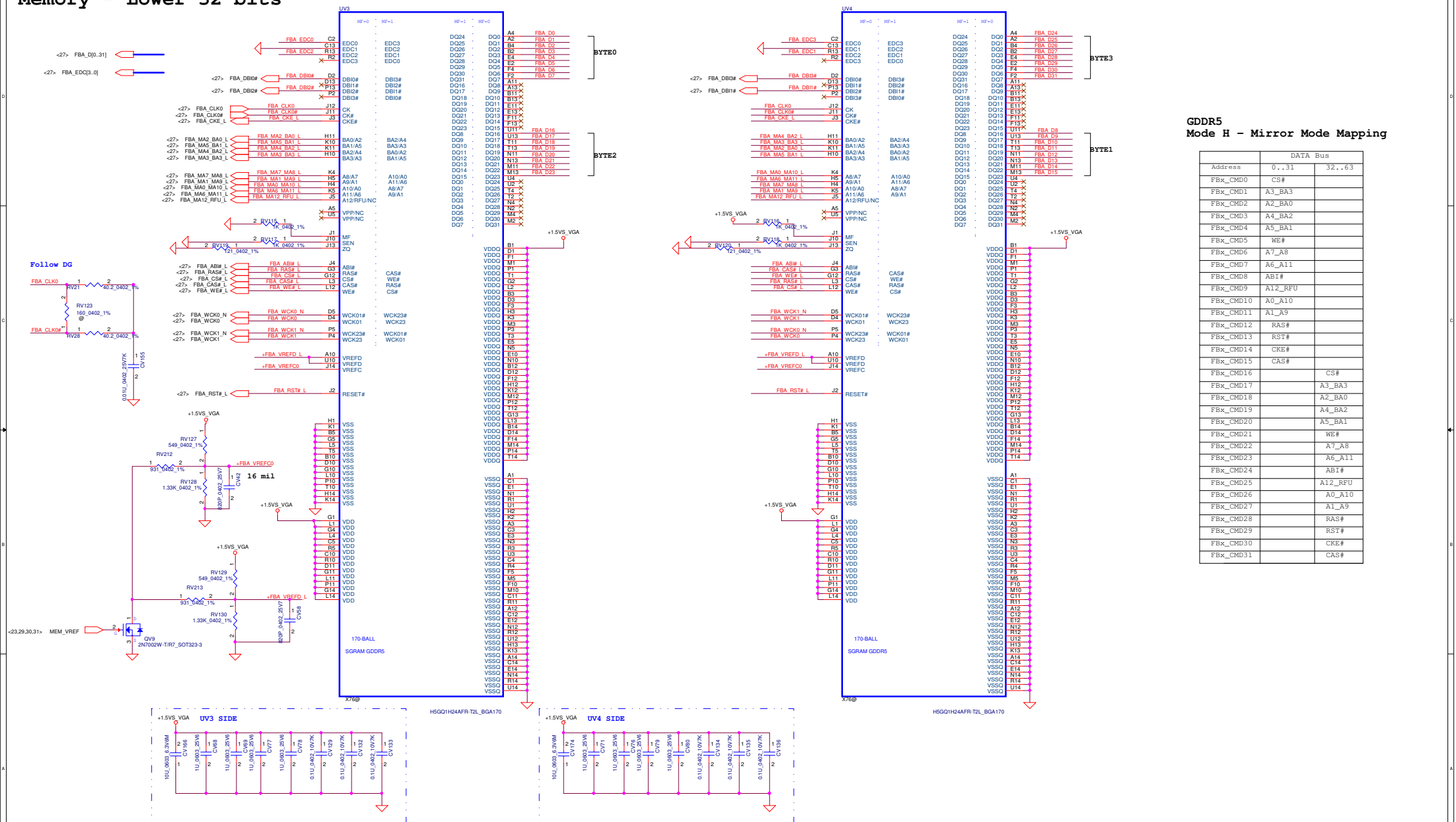


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Document Number	Y4005-NM-A141		Rev 1.0
Date	Monday, January 14, 2013	Sheet	23 of 65






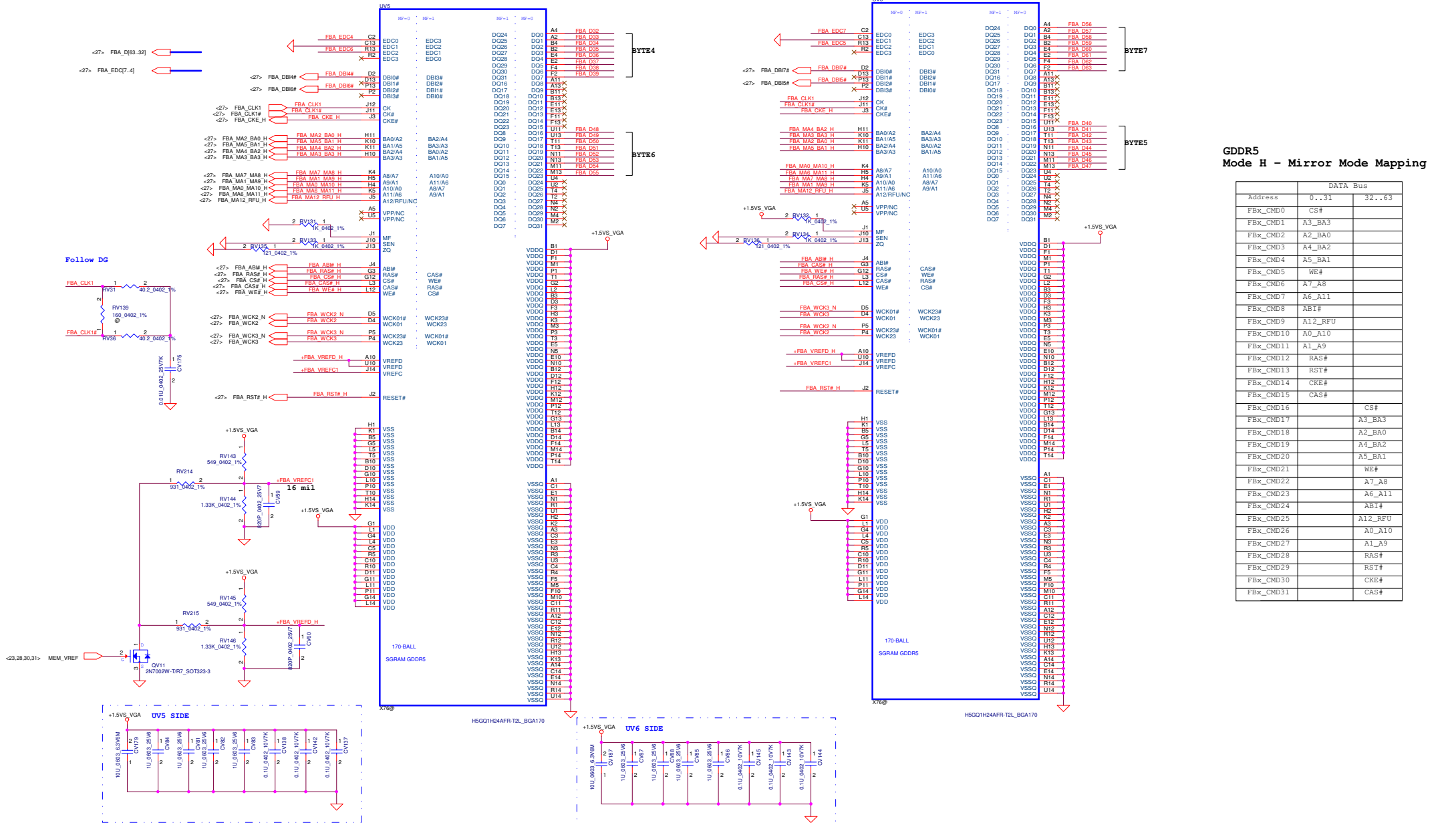
Memory - Lower 32 bits



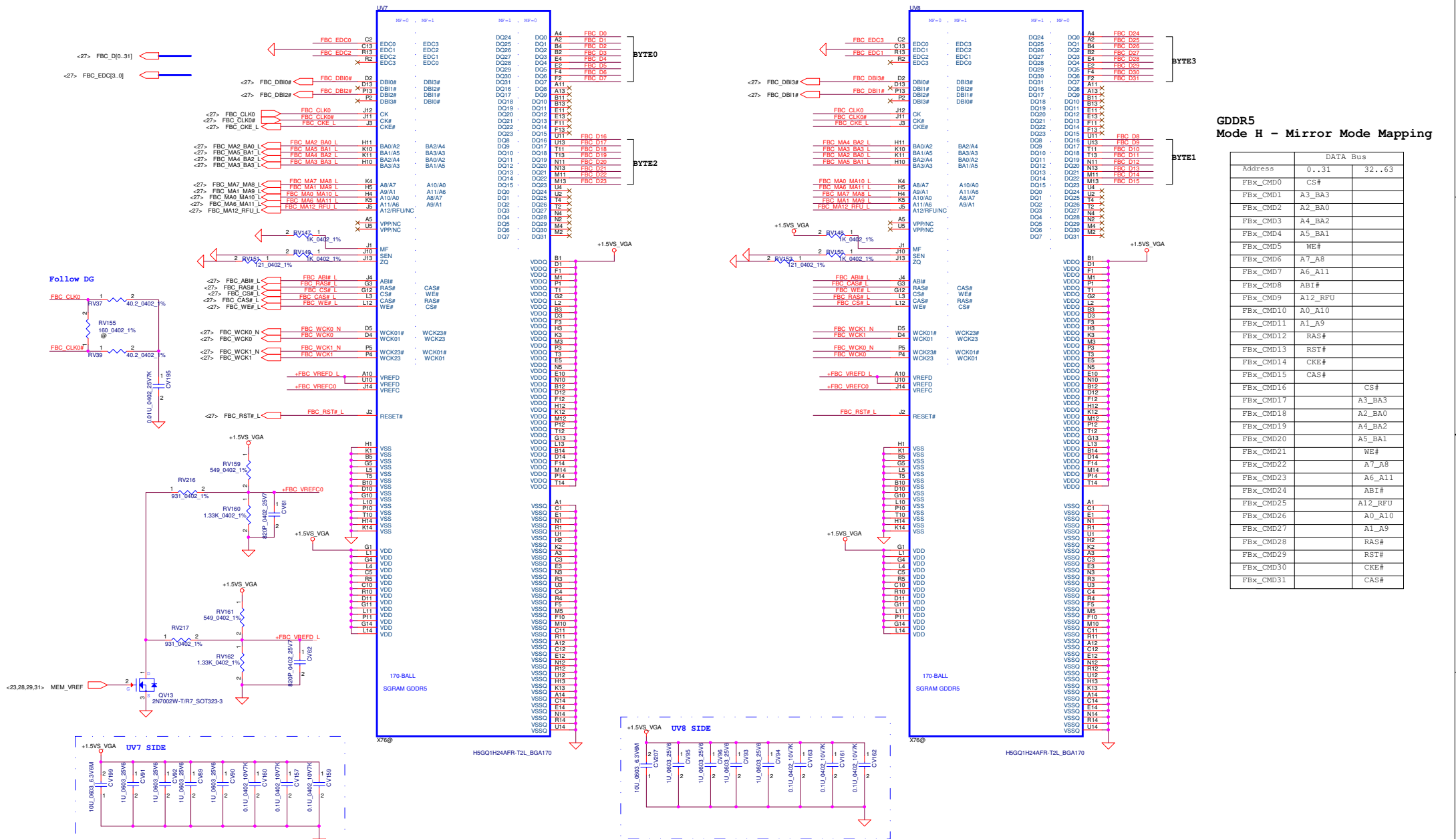
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	N14P-VRAM A Lower	
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Date: Monday, March 11, 2013				Signed: 28 of 65	

Memory - Upper 32 bits



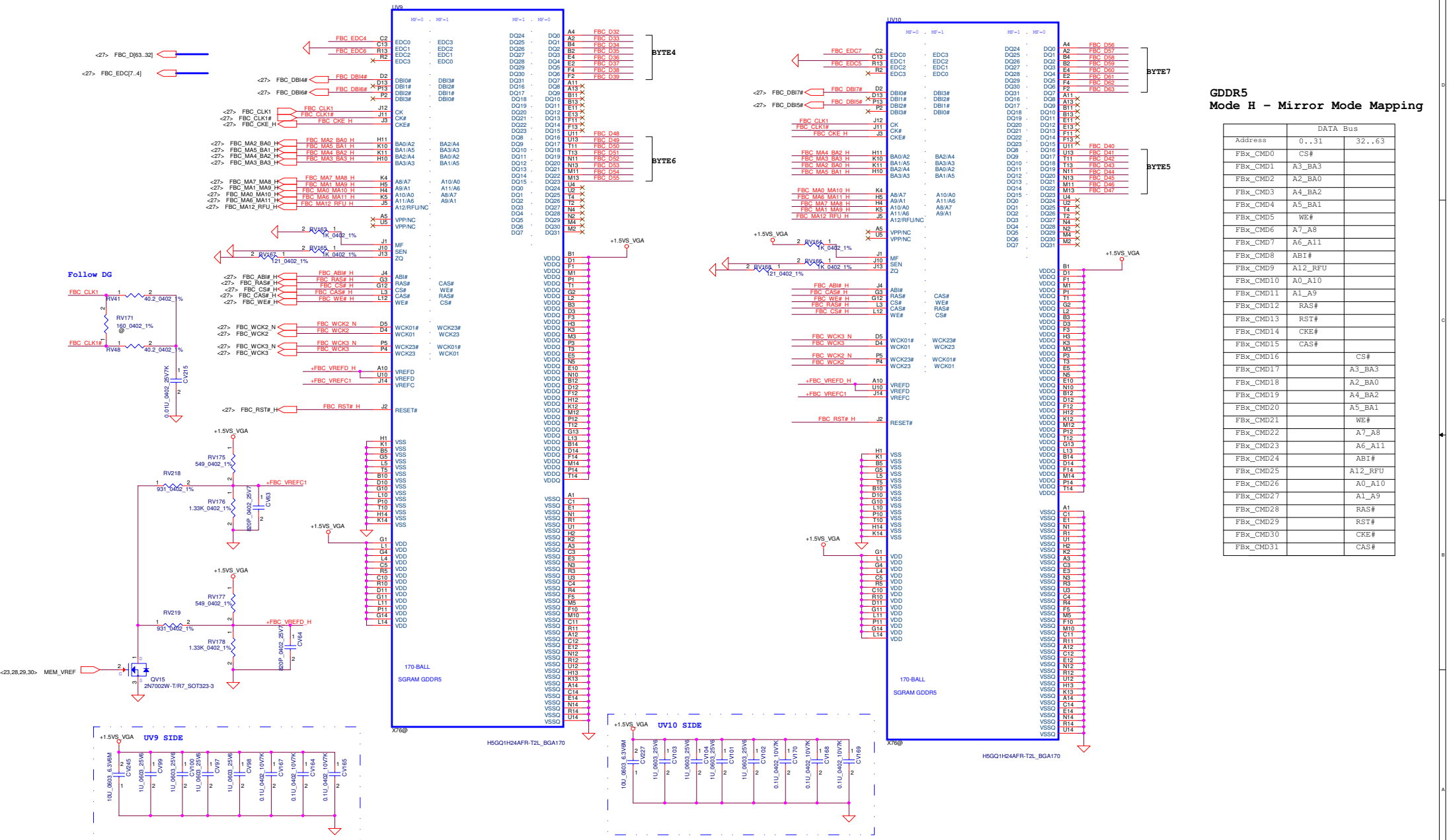
Memory Partition C - Lower 32 bits



GDDR5 Mode H - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
FBX_CMD0	CS#
FBX_CMD1	A3_BA3
FBX_CMD2	A2_BA0
FBX_CMD3	A4_BA2
FBX_CMD4	A5_BA1
FBX_CMD5	WE#
FBX_CMD6	A7_A8
FBX_CMD7	A6_A11
FBX_CMD8	AB1#
FBX_CMD9	A12_RFU
FBX_CMD10	A0_A10
FBX_CMD11	A1_A9
FBX_CMD12	RAS#
FBX_CMD13	RST#
FBX_CMD14	CKE#
FBX_CMD15	CAS#
FBX_CMD16	
FBX_CMD17	A3_BA3
FBX_CMD18	A2_BA0
FBX_CMD19	A4_BA2
FBX_CMD20	A5_BA1
FBX_CMD21	WE#
FBX_CMD22	A7_A8
FBX_CMD23	A6_A11
FBX_CMD24	AB1#
FBX_CMD25	A12_RFU
FBX_CMD26	A0_A10
FBX_CMD27	A1_A9
FBX_CMD28	RAS#
FBX_CMD29	RST#
FBX_CMD30	CKE#
FBX_CMD31	CAS#

Memory Partition C - Upper 32 bits



GDDR5 Mode H - Mirror Mode Mapping

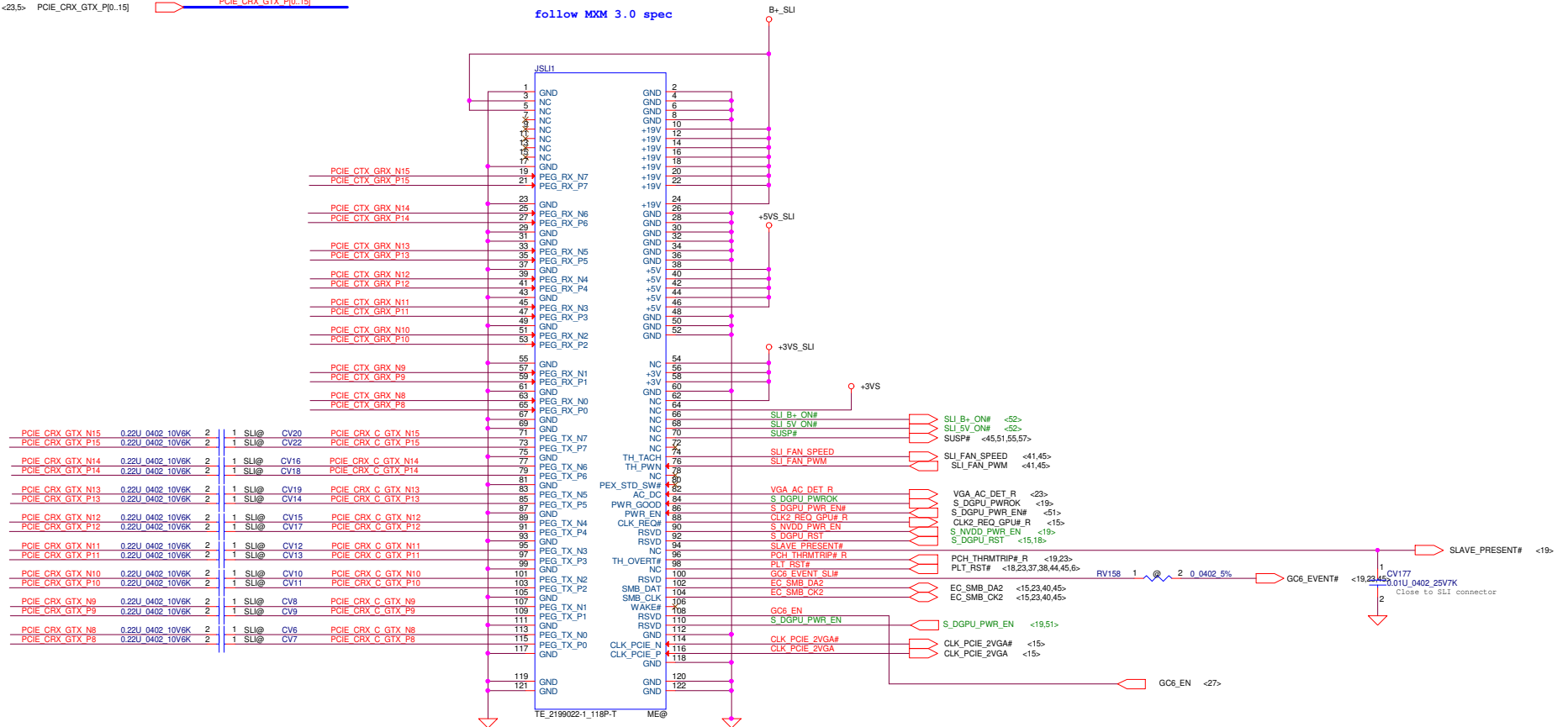
DATA Bus		
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#


11/11 for 2nd VGA fan
need to notice EC

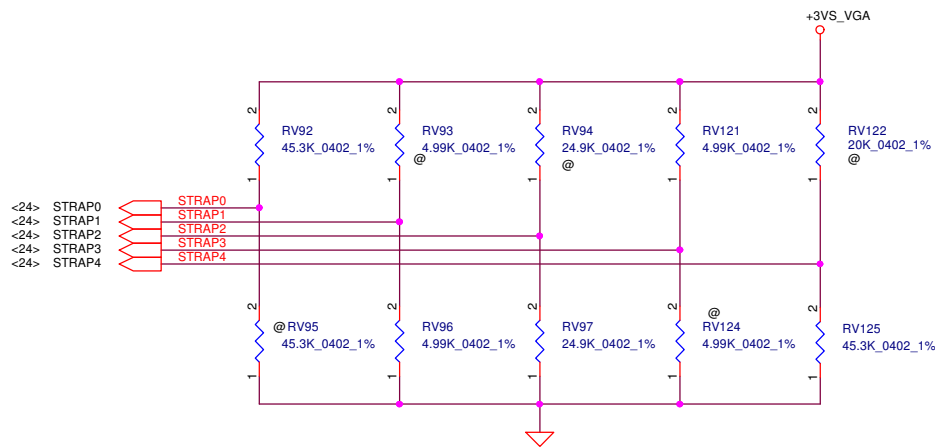
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<23.5> PCIE_CRX_GTX_P0..15]

PCIE_CTX_GRX_N0..15]
PCIE_CTX_GRX_P0..15]
PCIE_CRX_GTX_N0..15]
PCIE_CRX_GTX_P0..15]

follow MXM 3.0 spec



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						Custom		Y400S-NM-A141		1.0	
Date:		Monday, March 11, 2013		Sheet		32		of		65	



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

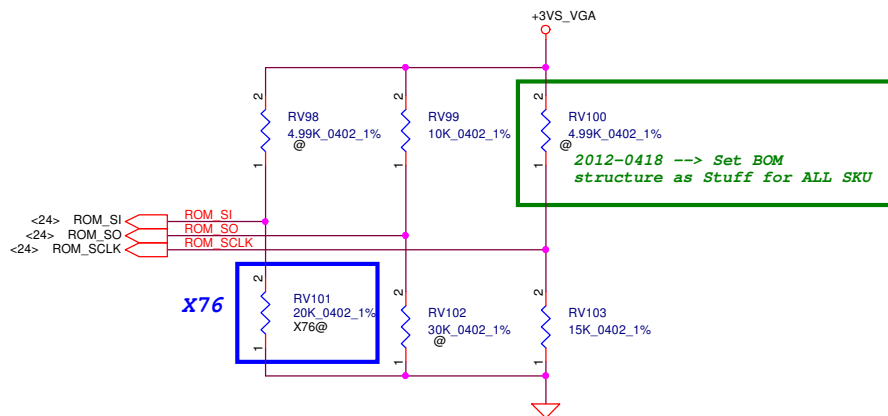
PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

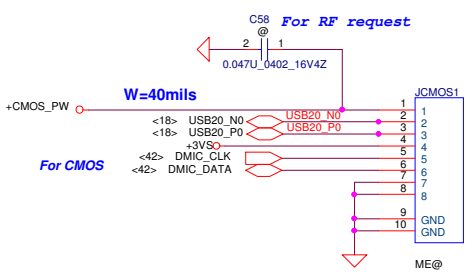
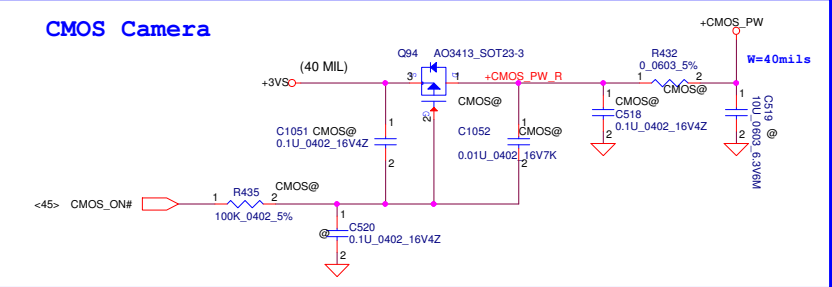
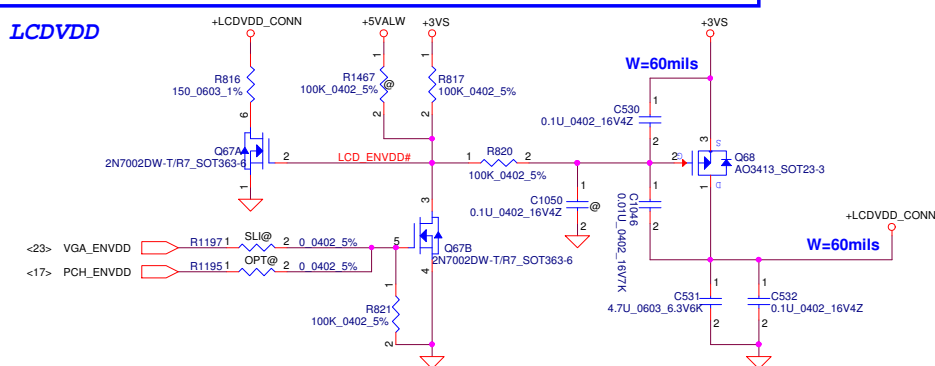
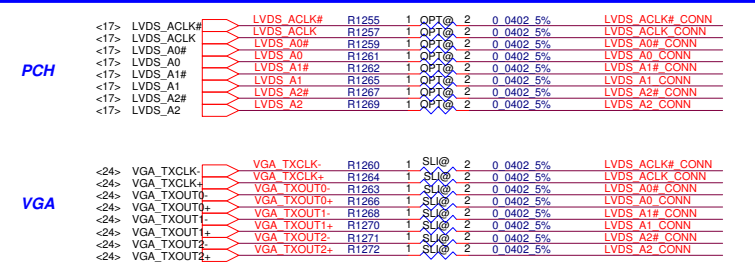
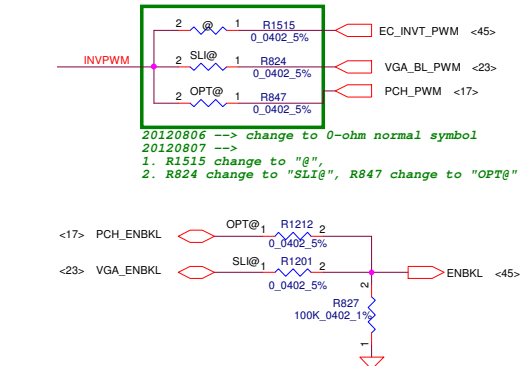
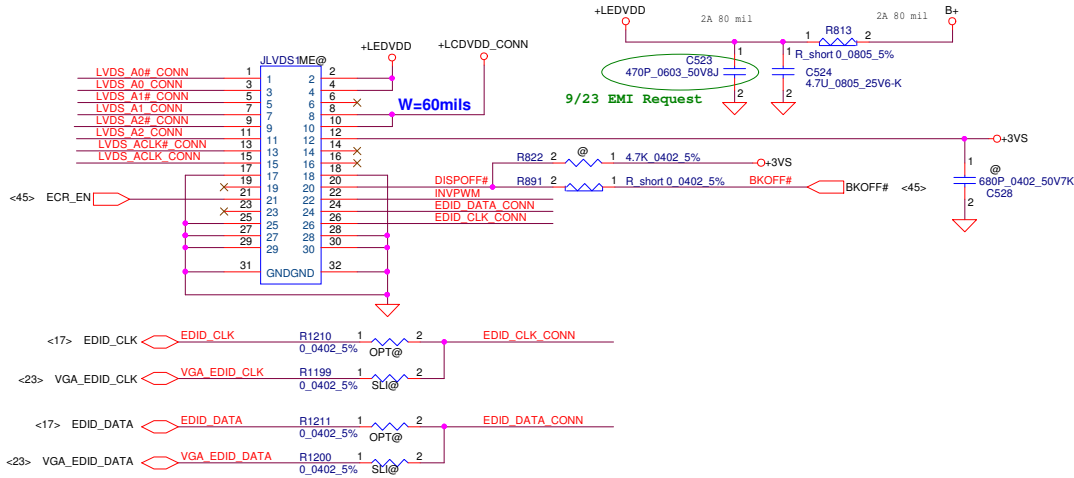
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)



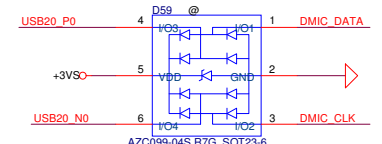
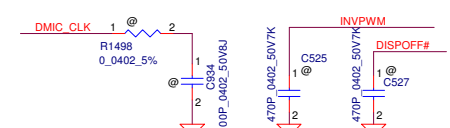
GPU		FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G 64Mx32		PD 30K	PU 10K	PU 35K (ALL SKU)	PU 45K	PD 5K	PD 25K	PU 5K	PD 45K
		K4G10325FG-HC04 1G 32Mx32		PD 45K							
	Hynix	H5GQ2H24MFR-T2C 2G 64Mx32	EOL	PD 25K							
		H5GQ1H24BFR-T2C 1G 32Mx32		PD 20K							
		H5GQ2H24AFR-T2C 2G 64Mx32		PD 5K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01 (2G 64Mx32)	SA00005B70J
	X76409JVL51 (1G 32Mx16)	SA00003RS0J
Hynix	X76409JVL02 (2G 64Mx32)	SA00004GD0J EOL
	X76409JVL02 (2G 64Mx32)	SA00004GD1J
	X76409JVL52 (1G 32Mx16)	SA00003WL1J

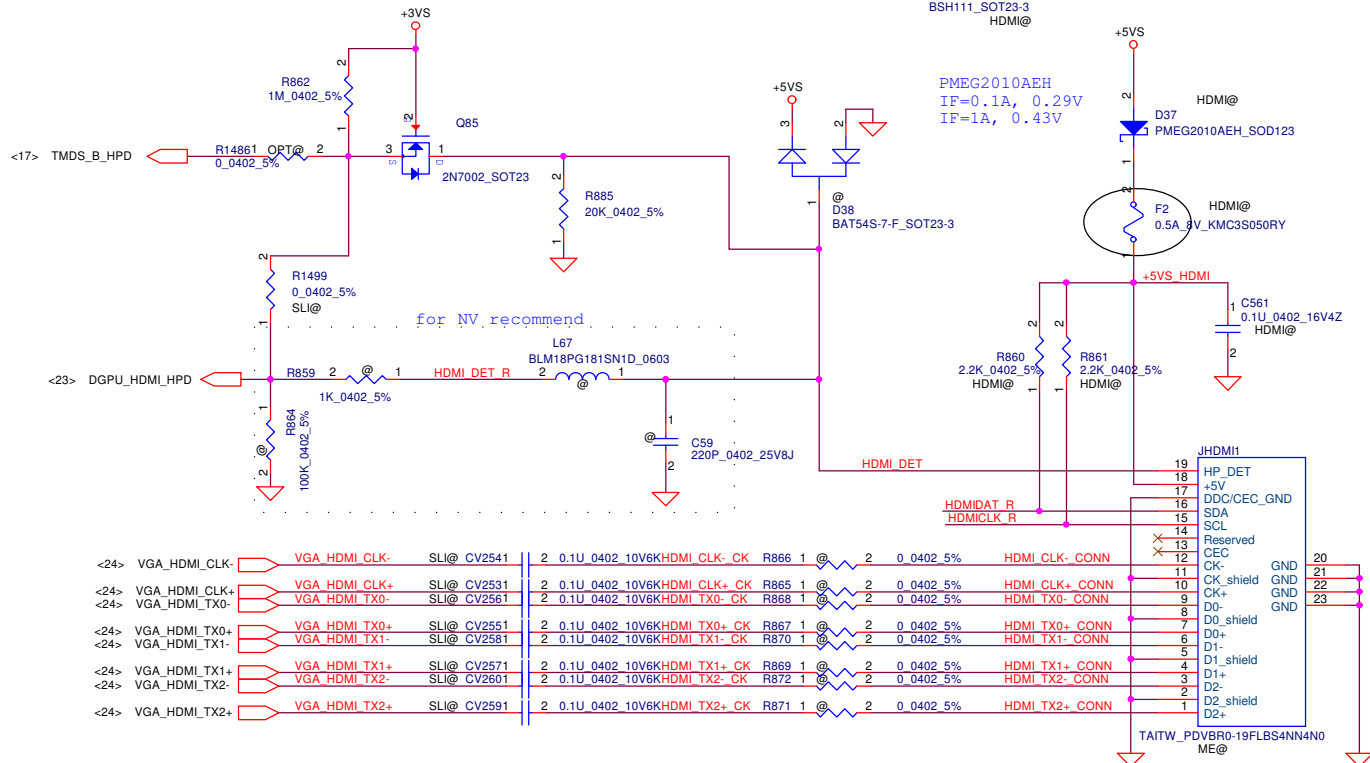
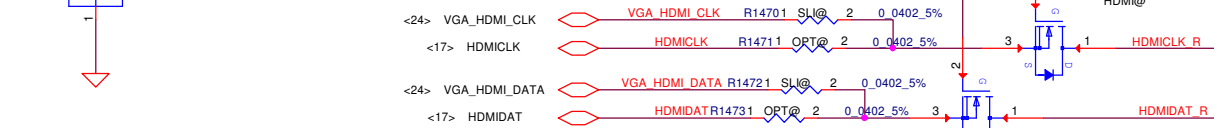
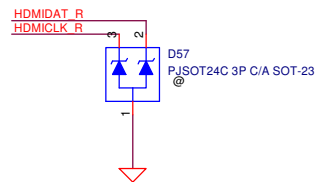
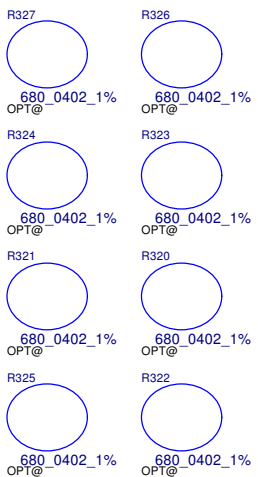
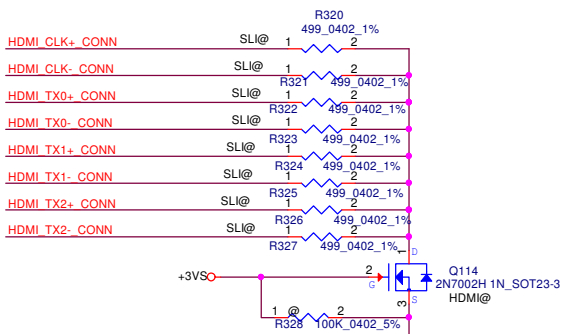
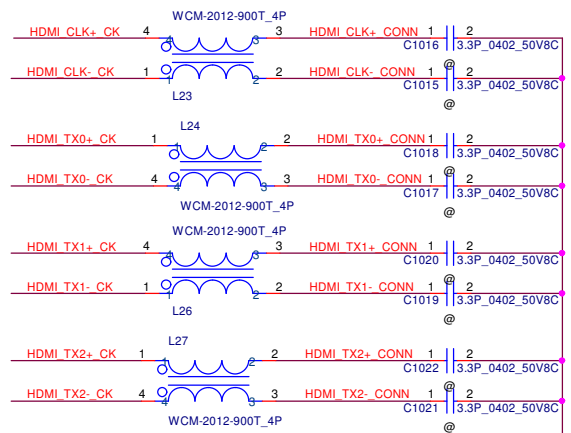
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	N14P_MISC	
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EMI request




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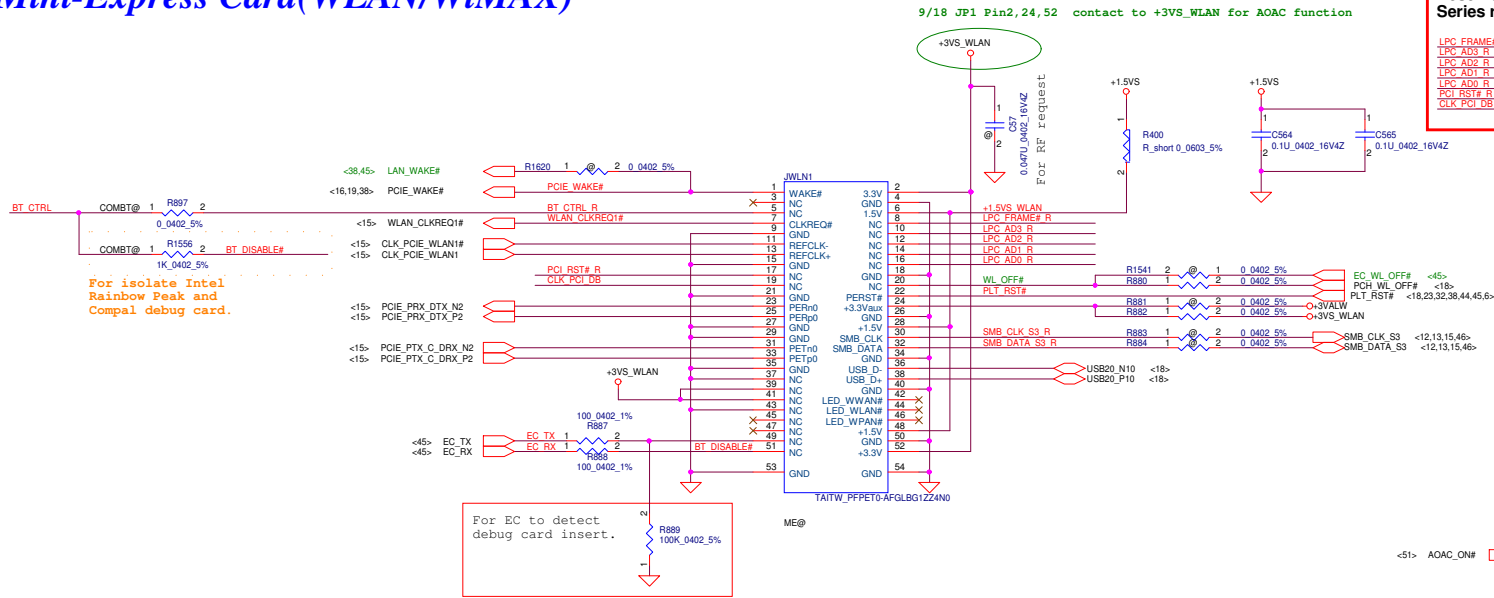
<17>	TMDS_B_DATA2#_PCH	TMDS_B_DATA2#_PCH	OPT@	C200	1	2	0.1U	0402	10V6K	HDMI TX2- CK	
<17>	TMDS_B_DATA2#_PCH	TMDS_B_DATA2#_PCH	OPT@	C201	1	2	0.1U	0402	10V6K	HDMI TX2+ CK	
<17>	TMDS_B_DATA1#_PCH	TMDS_B_DATA1#_PCH	OPT@	C202	1	2	0.1U	0402	10V6K	HDMI TX1- CK	
<17>	TMDS_B_DATA1#_PCH	TMDS_B_DATA1#_PCH	OPT@	C203	1	2	0.1U	0402	10V6K	HDMI TX1+ CK	
<17>	TMDS_B_DATA0#_PCH	TMDS_B_DATA0#_PCH	OPT@	C204	1	2	0.1U	0402	10V6K	HDMI TX0- CK	
<17>	TMDS_B_DATA0#_PCH	TMDS_B_DATA0#_PCH	OPT@	C205	1	2	0.1U	0402	10V6K	HDMI TX0+ CK	
<17>	TMDS_B_CLK#_PCH	TMDS_B_CLK#_PCH	OPT@	C206	1	2	0.1U	0402	10V6K	HDMI TX0- CK	
<17>	TMDS_B_CLK#_PCH	TMDS_B_CLK#_PCH	OPT@	C207	1	2	0.1U	0402	10V6K	HDMI TX0+ CK	



HDMI W/O Logo: R00000001HM

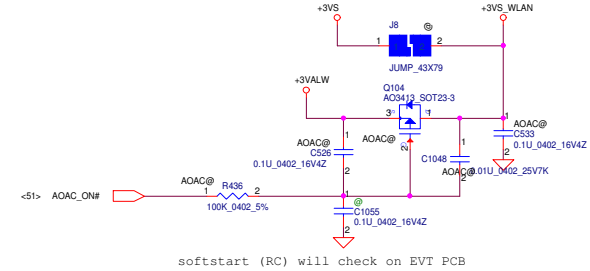
Security Classification		LC Future Center Secret Data				Title			
Issued Date		2011/11/01		Deciphered Date		2012/12/31			
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Mini-Express Card(WLAN/WiMAX)

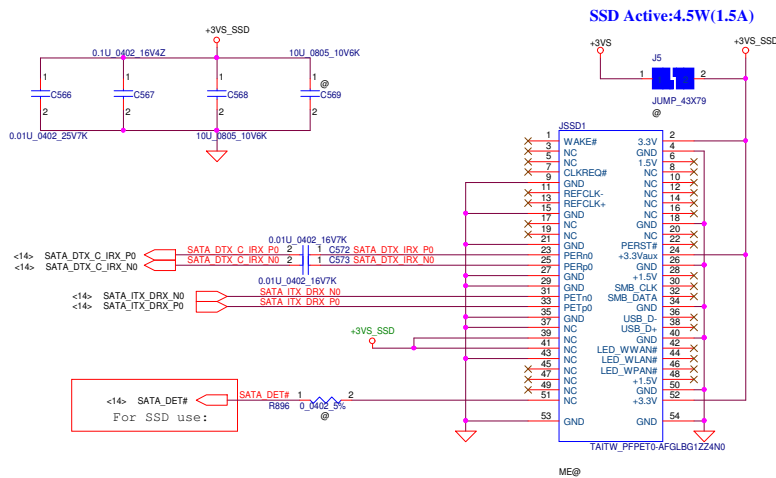


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC FRAME# R	R873	1	2	0.0402 5%	LPC FRAME#	LPC FRAME#	<14,45>
LPC AD3 R	R874	1	2	0.0402 5% <td>LPC AD3</td> <td>LPC AD3</td> <td><14,45></td>	LPC AD3	LPC AD3	<14,45>
LPC AD2 R	R875	1	2	0.0402 5% <td>LPC AD2</td> <td>LPC AD2</td> <td><14,45></td>	LPC AD2	LPC AD2	<14,45>
LPC AD1 R	R876	1	2	0.0402 5% <td>LPC AD1</td> <td>LPC AD1</td> <td><14,45></td>	LPC AD1	LPC AD1	<14,45>
LPC AD0 R	R877	1	2	0.0402 5% <td>LPC AD0</td> <td>LPC AD0</td> <td><14,45></td>	LPC AD0	LPC AD0	<14,45>
CLK_P0T_08	R878	1	2	0.0402 5% <td>CLK_P0T_08</td> <td>CLK_P0T_08</td> <td><18></td>	CLK_P0T_08	CLK_P0T_08	<18>

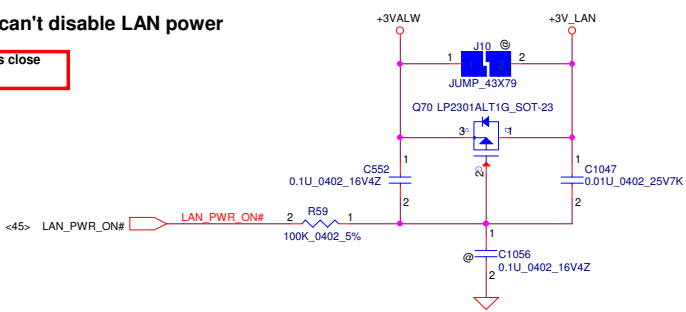


Mini-Express Card(SSD)

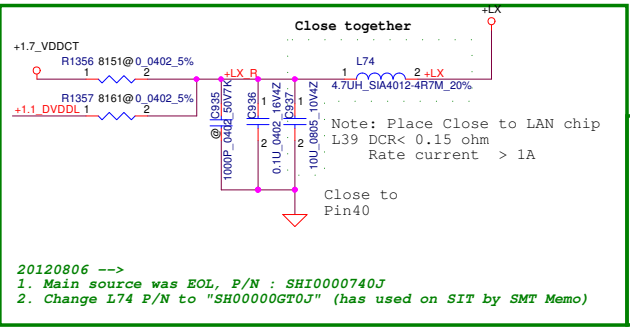
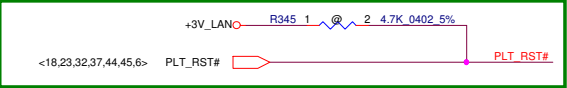


Atheros request can't disable LAN power

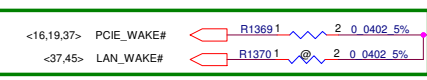
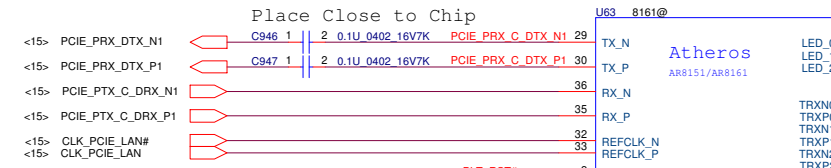
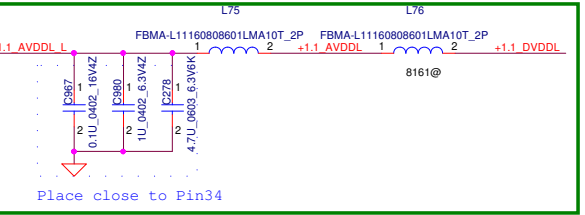
Layout Notice : Place as close chip as possible.



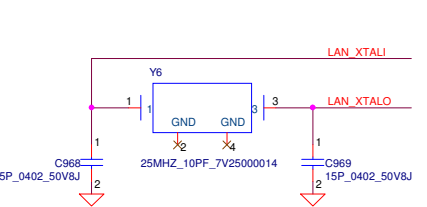
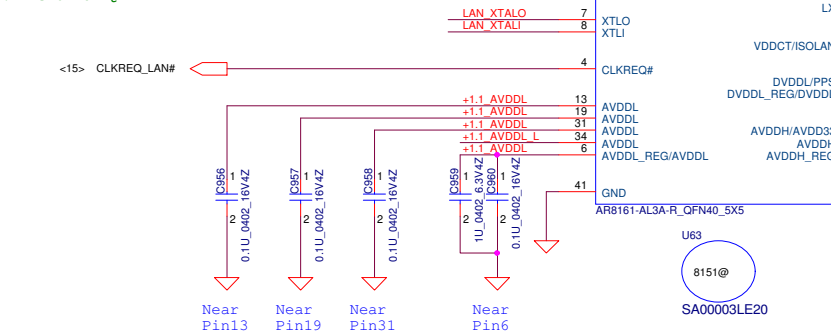
Vendor recommend reseve the PU resistor close LAN chip



	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356, C955
AR8161	+1.1V <DVDDL, AVDDL>	R1357, R1372, L76

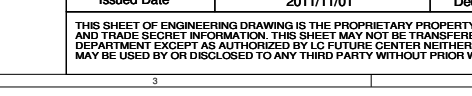
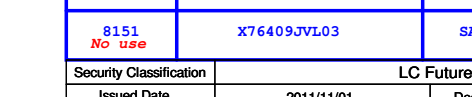
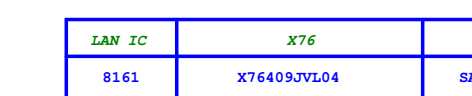
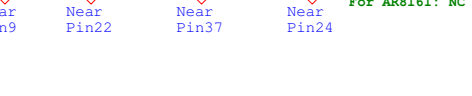
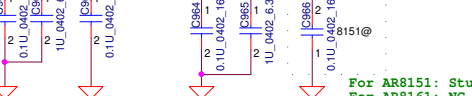
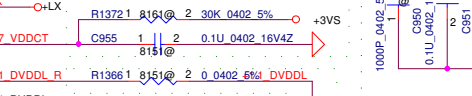
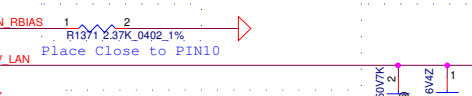
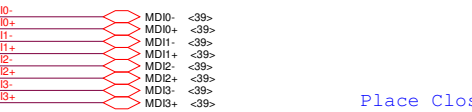
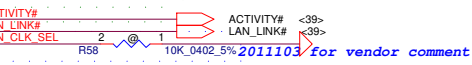


20120718 --> for LAN wakeup backlight issue
1. R1369 to "Mount"
2. R1370 to "g"

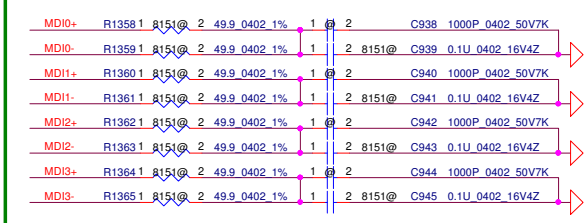


20120816 -->
1. change P/N to 7V2500014(10pf), SJ10000E80J

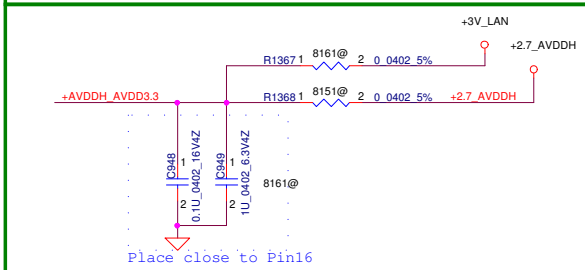
H --> Overclocking mode
L --> Not overclocking mode



Place Close to LAN chip



Note : C938, C940, C942, 944, reserved for EMI.
For AR8151: Stuff 49.9K and 0.1u
For AR8161: NC

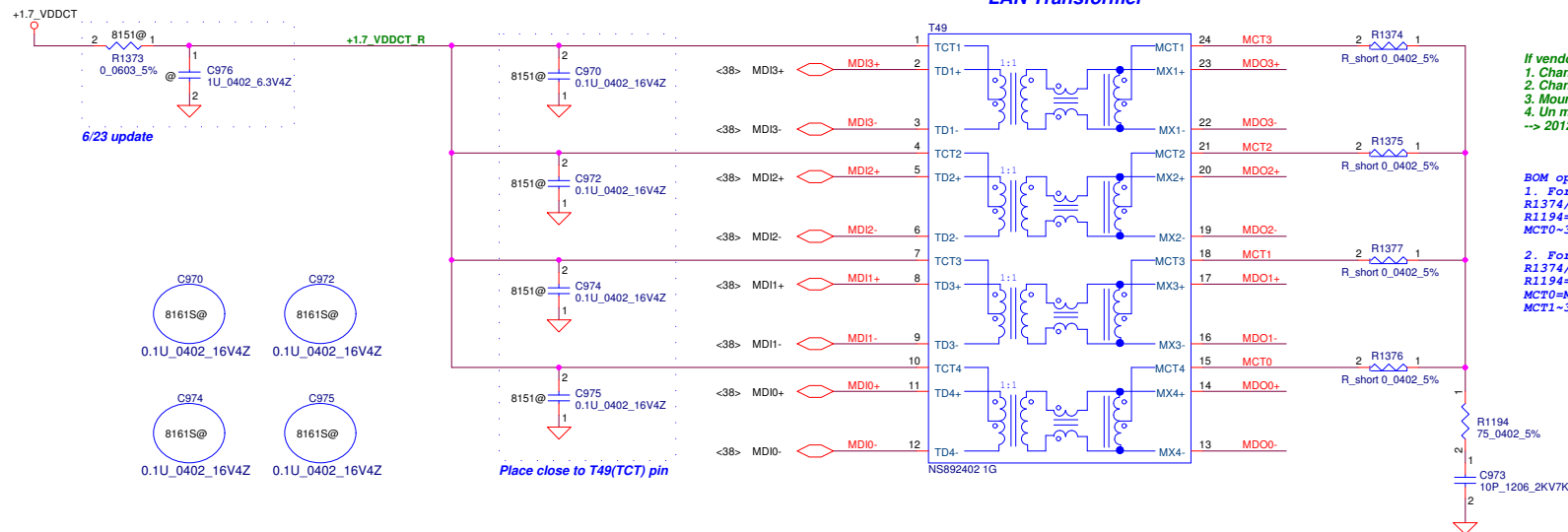


For AR8151: Stuff R1368 for +AVDD3.3
For AR8161: Stuff R1367, C949 for +AVDDH

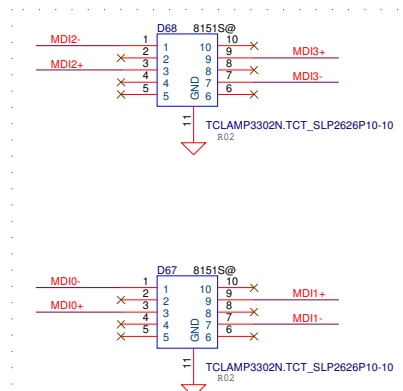
LAN IC	X76	VRAM P/N
8161	X76409JVL04	SA000050E1J
8151 No use	X76409JVL03	SA00003LE2J

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Title				LAN-AR8151/8161			
Size		Document Number		Y400S-NM-A141		Rev 1.0	
Date		Monday, March 11, 2013		Sheet 38		of 65	

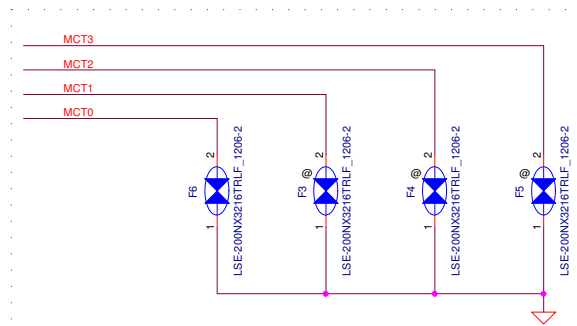


Place Close to T49



Reserve D67, D68 for EMI go rural solution

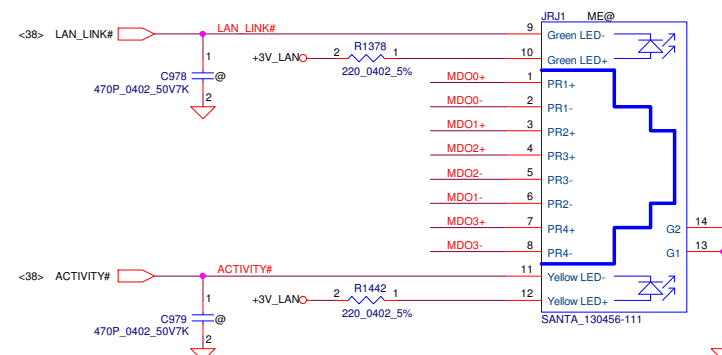
Place Close to T49

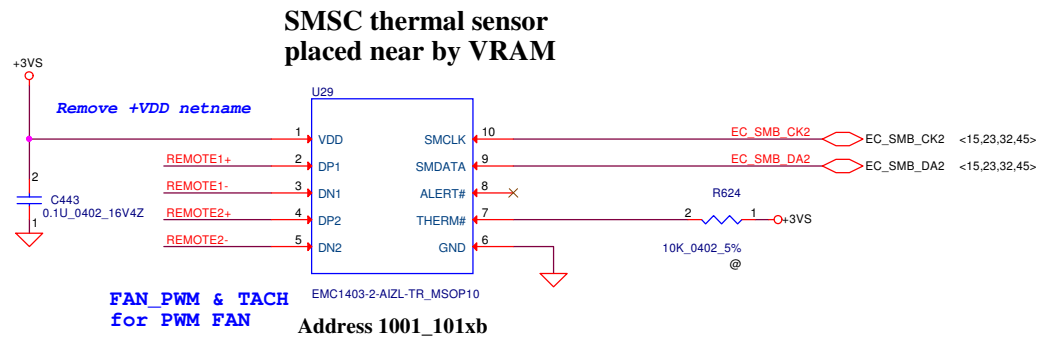
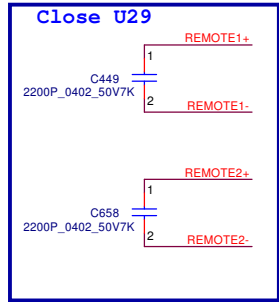


Reserve for EMI go rural solution

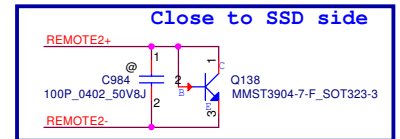
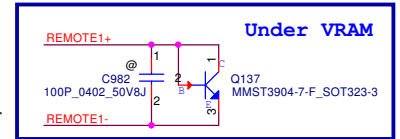
2012-0622 -->
 1. Change the BOM Structure of LAN SURGE to "@" --> F3, F4, F5
 2. Del SURGE@ on Y400 BOM, and change the BOM structure of F6 to "Stuff"
 20120807 -->
 1. Change Lan Surge P/N to "SCV00001F0J" to meet DC400V Lenovo spec
 2. Only change P/N(F3,F4,F5 and F6), not used correct symbol.

LAN Conn.



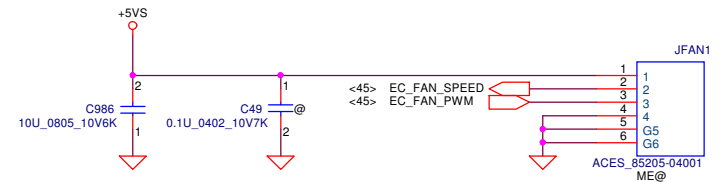


internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp



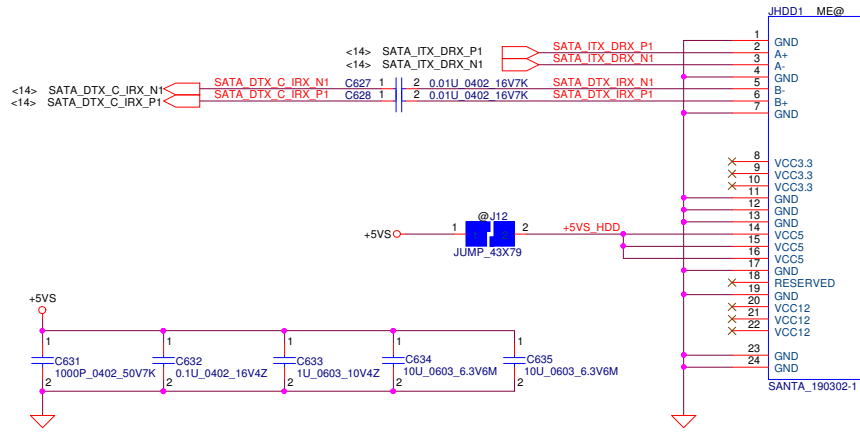
REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn

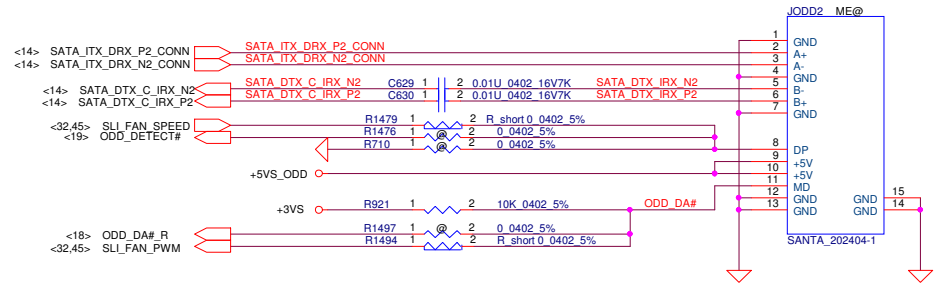


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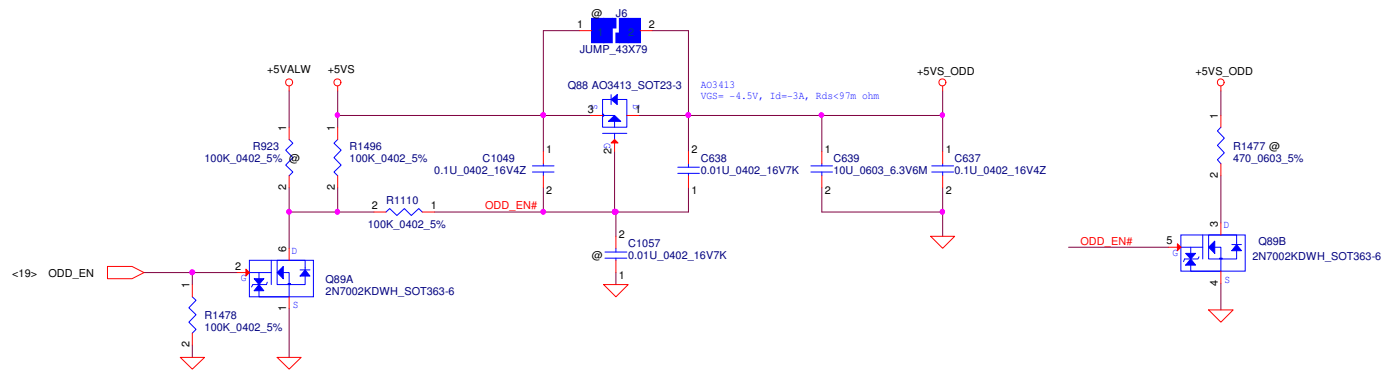
SATA HDD Conn.

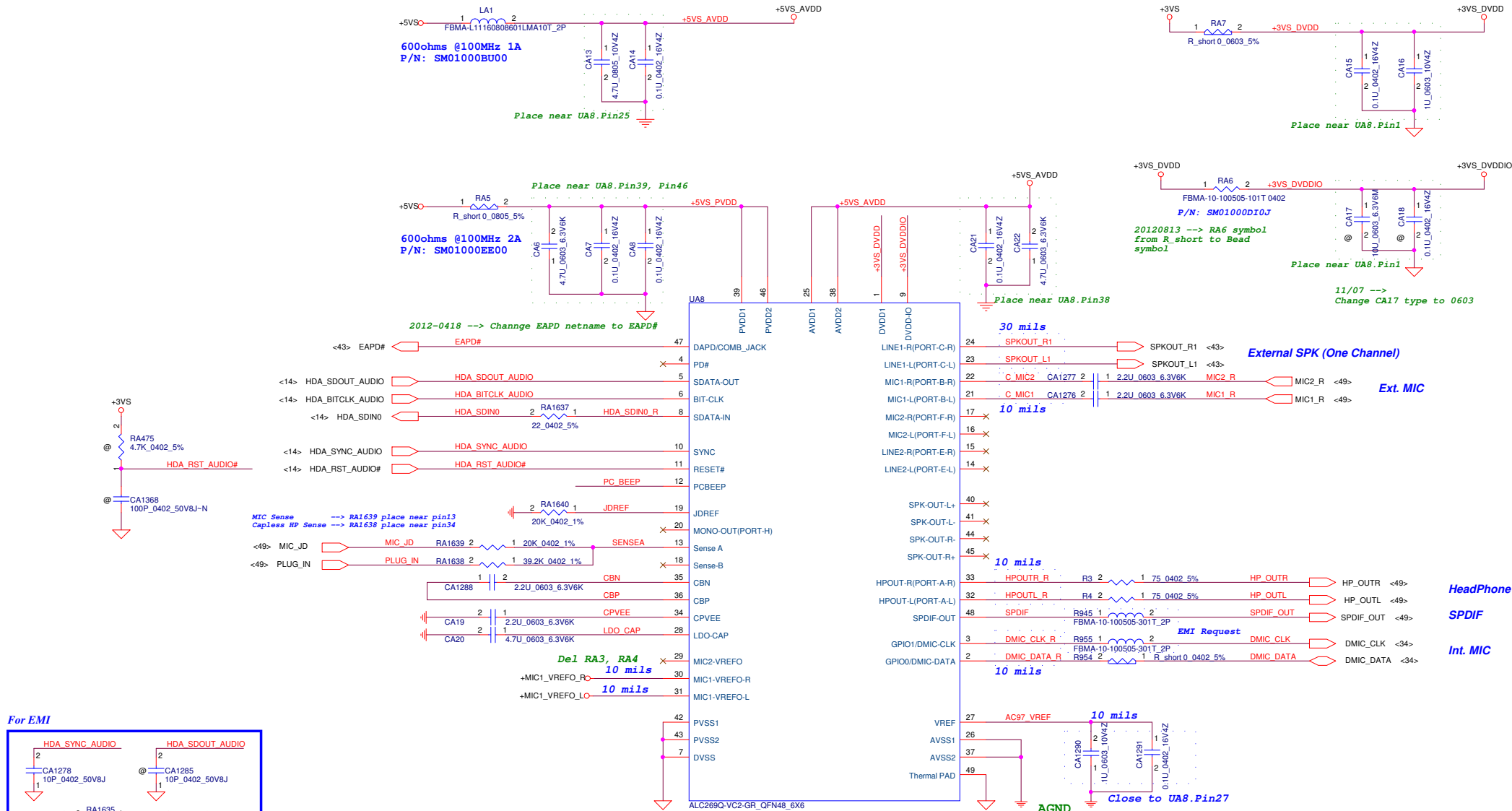


SATA ODD Conn.

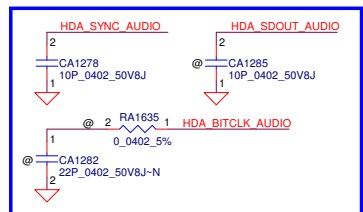


ODD Power Control

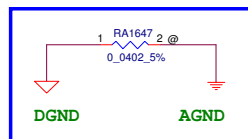
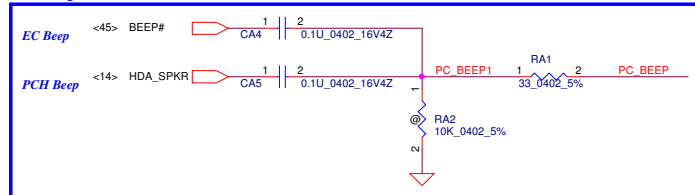




For EMI

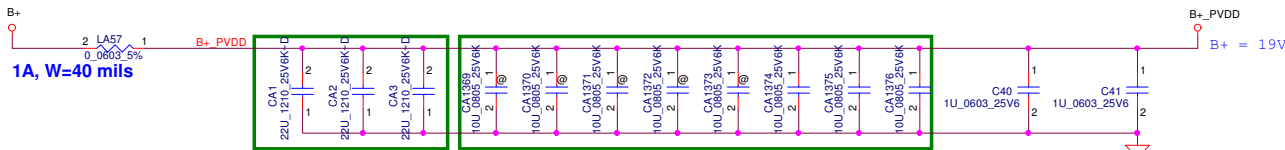


PC Beep

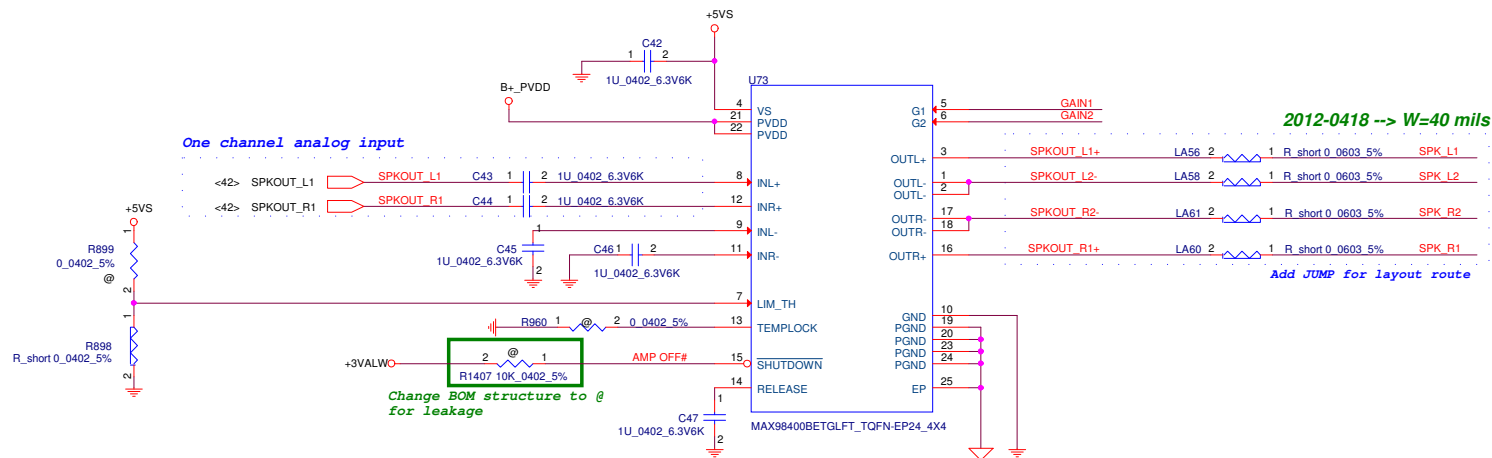


Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1 (Pin21/22)	External	Mic in

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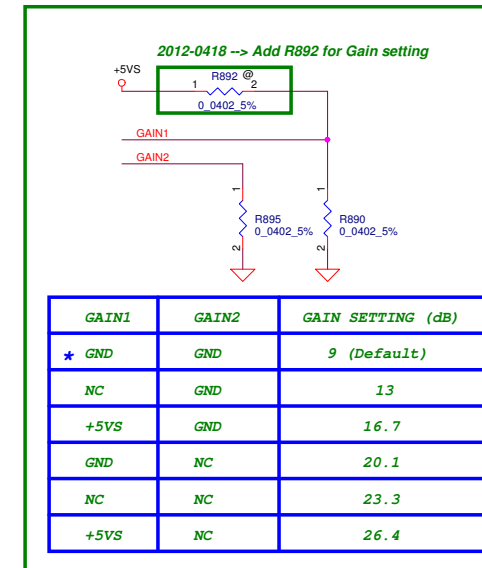
22uF*3, 10uF*8 for Damage issue
Stuff --> CA1, CA2, CA3, CA1374, CA1375 and CA1376



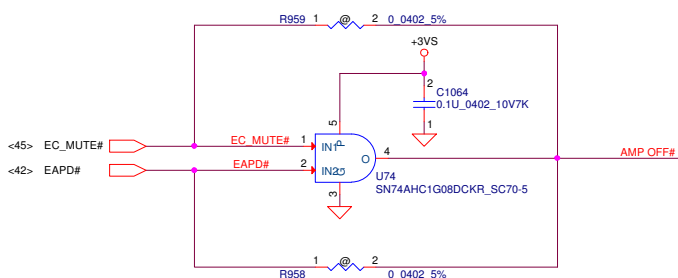
2012-0418 --> W=40 mils

2012-0429 --> Change C42-C47 Cap to X5R type for Vendor suggestion

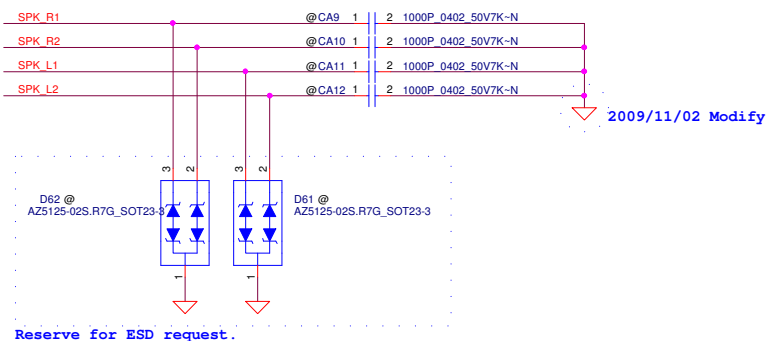
GAIN SETTING



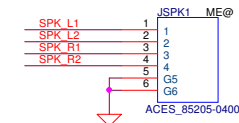
2012-0418 --> Set R890 BOM structure as Stuff

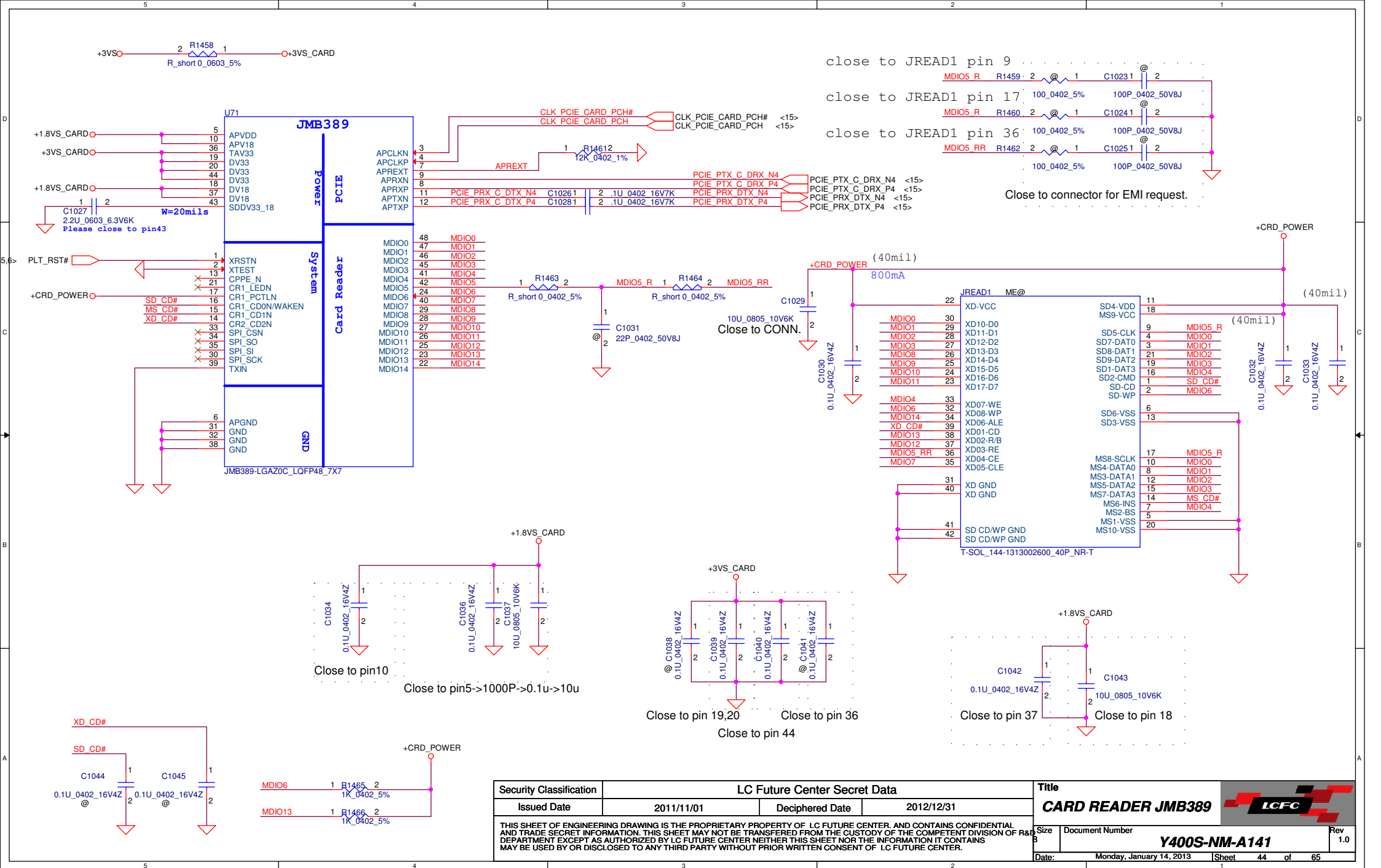


2012-0622 --> change these BOM structure for BOBO noise issue
1. R958, R959 --> "UnStuff"
2. U74, C1064 --> "Stuff"



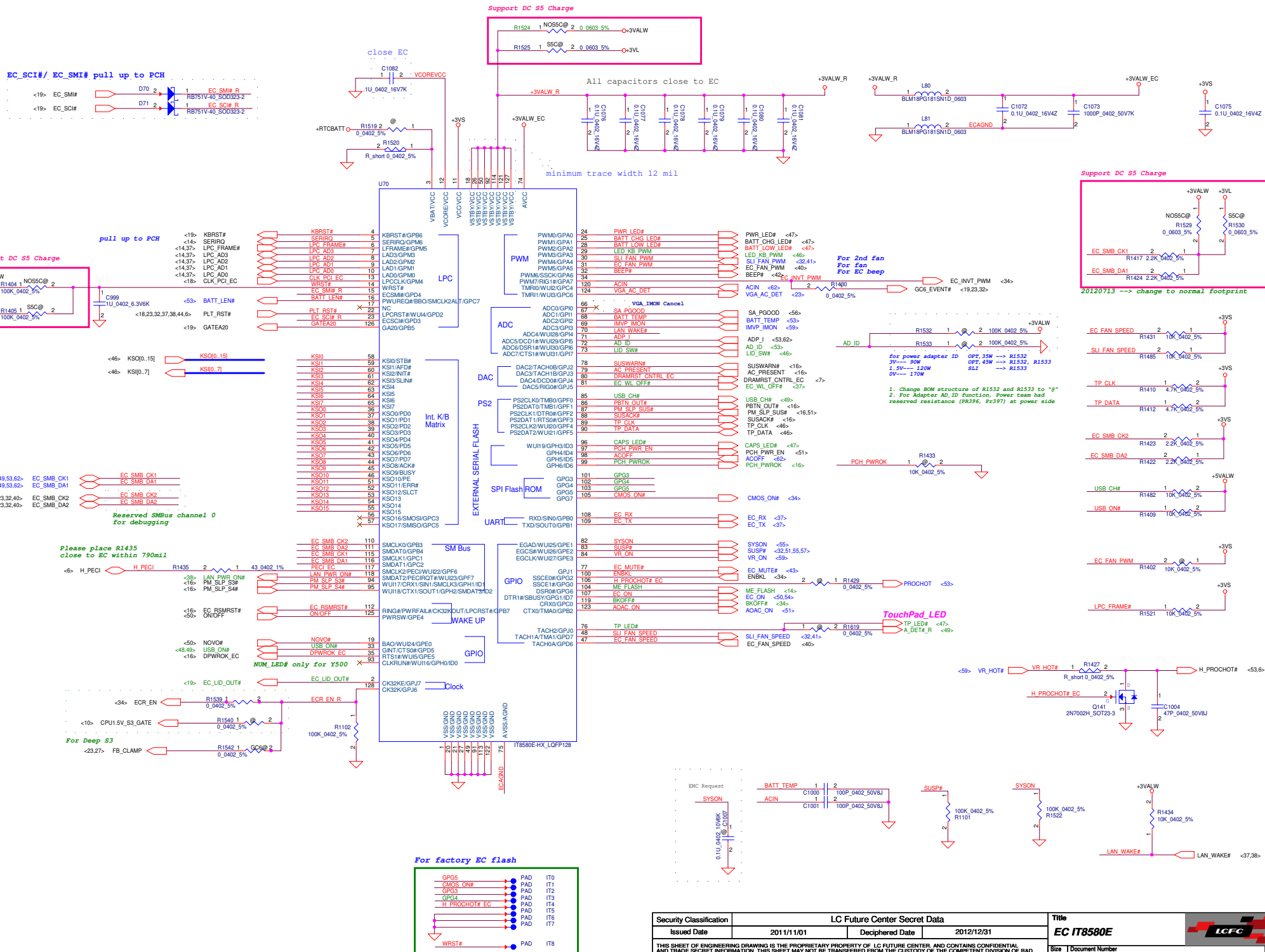
Speaker Conn.



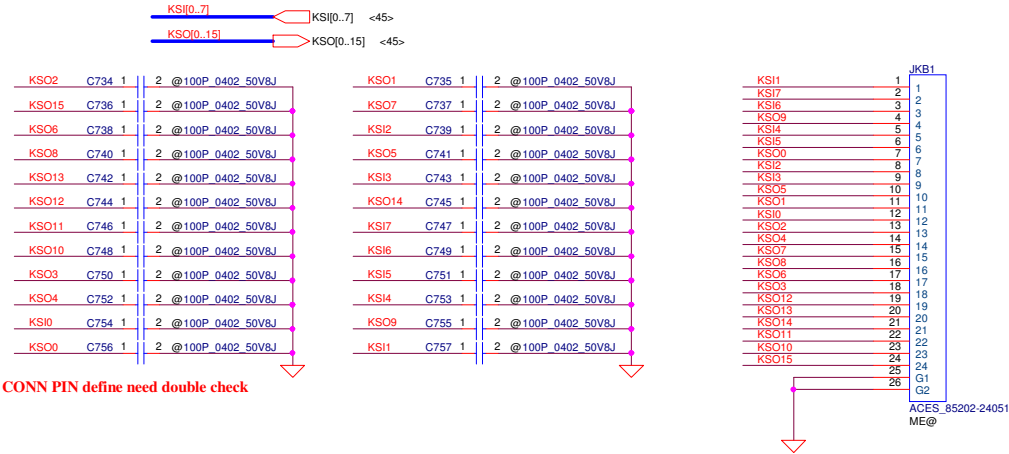


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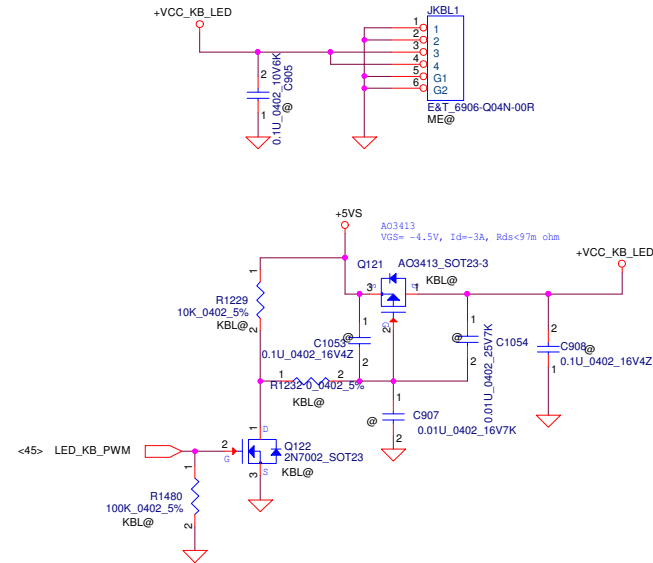
Title		LCFC	
CARD READER JMB389			
Size	Document Number	Y400S-NM-A141	
Date:	Monday, January 14, 2013	Sheet	44 of 65
		Rev	1.0



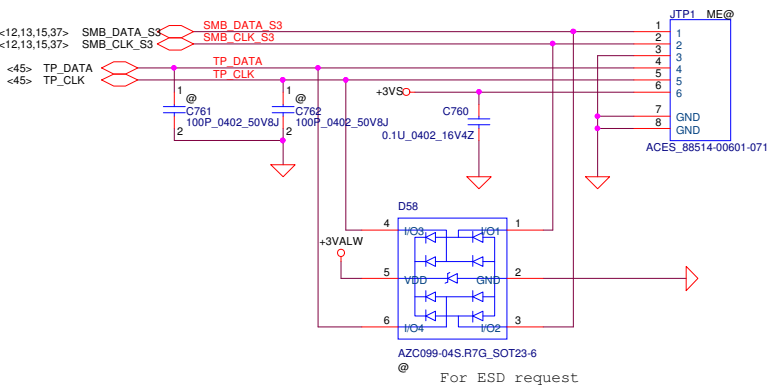
14" INT_KBD Conn.



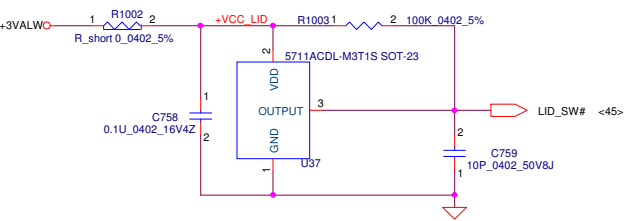
KB Lighting CONN.4pin

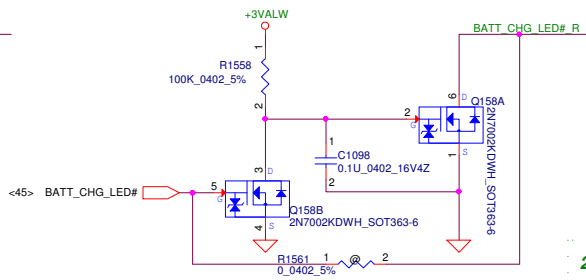
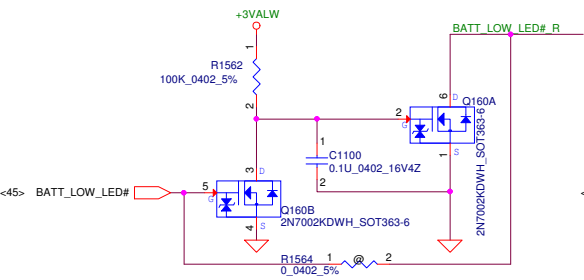


To TP/B Conn.

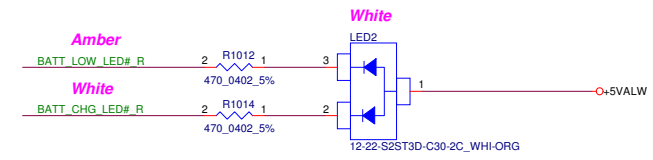


Lid Switch

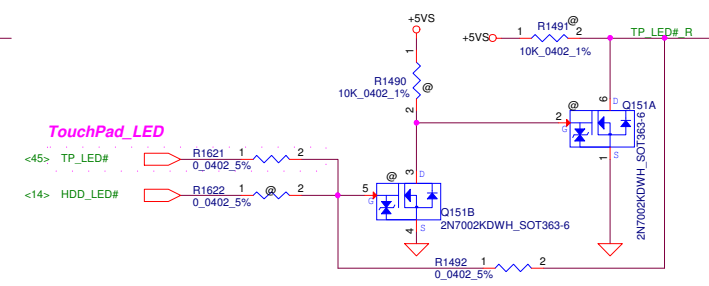
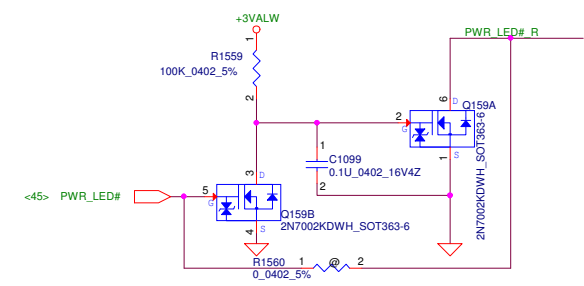




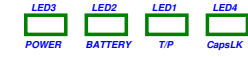
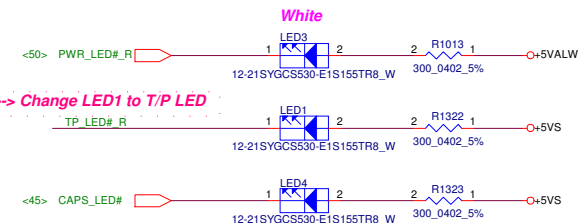
BATT CHARGE/LOW LED



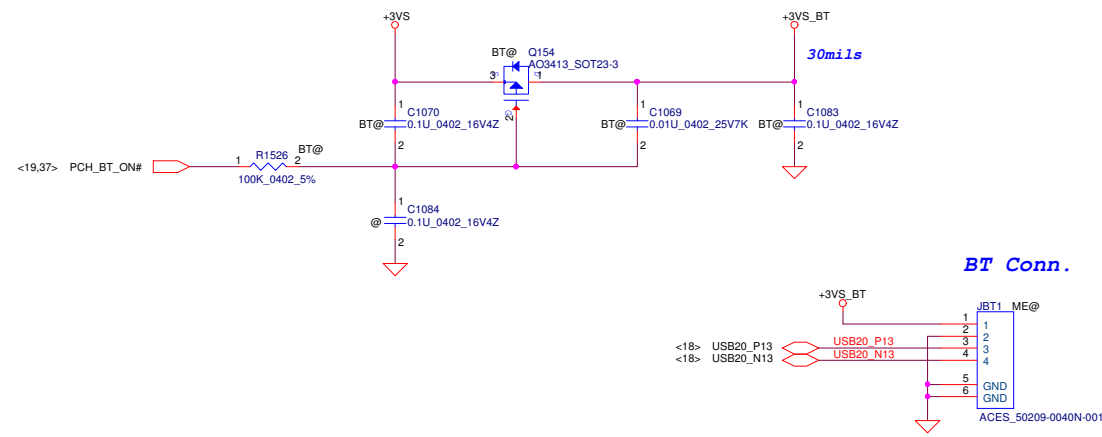
2012-0507 --> Add MOS solution onLED3, 2 to avoid the light blinked.



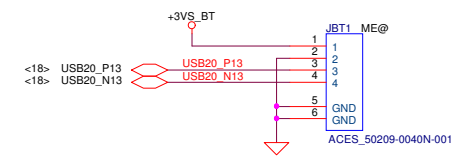
PWR LED HDD LED CapsLK LED



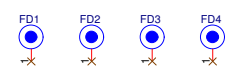
BlueTooth DC



BT Conn.

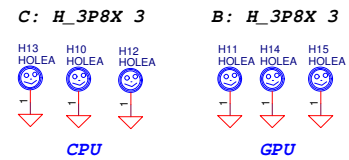


PCB Federal Mark PAD

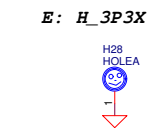


Screw Hole

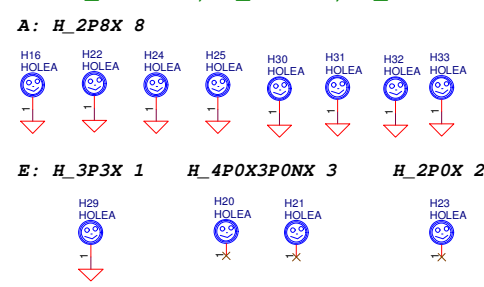
CPU and GPU: H_3P8X 6



MIN PCIE: H_3P3 X 1



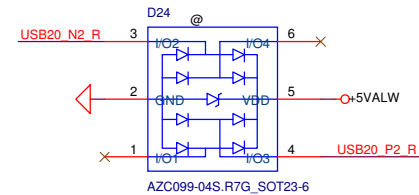
ME: H_8P0 X 8; H_3P3X 1; H_4P0X3P0N X 2; H_2P0X 1




Security Classification		LC Future Center Secret Data		Title	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	LED/EC SPI ROM/BT	
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				Custom	Y400S-NM-A141
				Date:	Monday, January 14, 2013
				Sheet	47 of 65

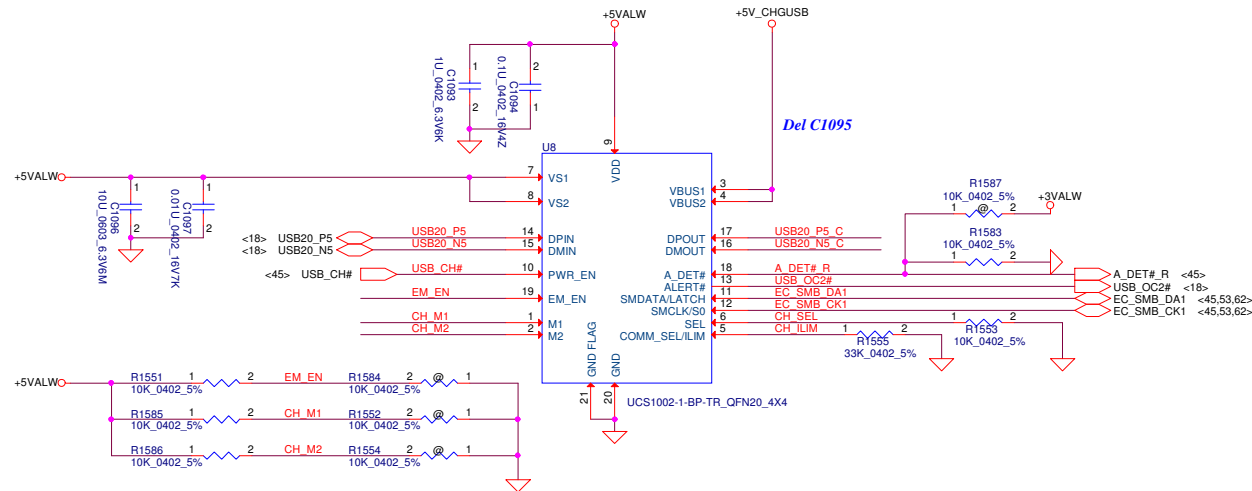
The diagram shows the USB_OC1# pin configuration. A pull-up resistor C767 (0.1uF) is connected to +5VALW and the USB_ON# pin of the U39 (G547I2P81U_MSOP8) chip. The chip's VOUT pin is connected to the USB_OC1# pin, which is also pulled up to +USB_VCCA by resistor C904 (1000P_0402_50V7K). The chip's EN pin is connected to GND. The chip is labeled 'Low Active 2A'.

Three schematic diagrams showing USB signal connections for L68, L70, and L72. Each diagram shows a 4-pin connector with red and blue wires. L68: USB30_RX_N3 (2) to USB30_RX_R_N3 (1), USB30_RX_P3 (3) to USB30_RX_R_P3 (4). L70: USB30_TX_C_N3 (2) to USB30_TX_R_N3 (1), USB30_TX_C_P3 (3) to USB30_TX_R_P3 (4). L72: USB20_N2 (2) to USB20_N2_R (1), USB20_P2 (3) to USB20_P2_R (4). All diagrams are labeled WCM-2012-900T_4P.



Title			
USB3.0 PORT			
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		Rev	1.0

Sleep & Charge Right side USB Charger Port (USB_Port5, near JMIC1)



2012-0429 --> Set default mode is "BC1.2 CDP" Mode (2.5A on S0) for USB Port5

Active Mode Selection:

M1	M2	EM_EN	ACTIVE MODE
0	0	1	Dedicated Charger Emulation Cycle
0	1	0	Date Pass-Through
0	1	1	BC1.2 DCP
1	0	0	BC1.2 SDP
1	0	1	Dedicated Charger Emulation Cycle
1	1	0	Date Pass-Through
★ 1	1	1	BC1.2 CDP

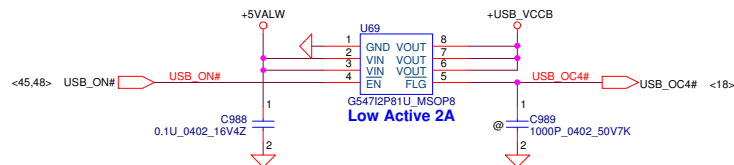
ILIM SETTING

Pull Low
0R-500mA
10K-900mA
12K-1000mA
15K-1200mA
18K-1500mA
22K-1800mA
27K-2000mA
★ 33K-2500mA

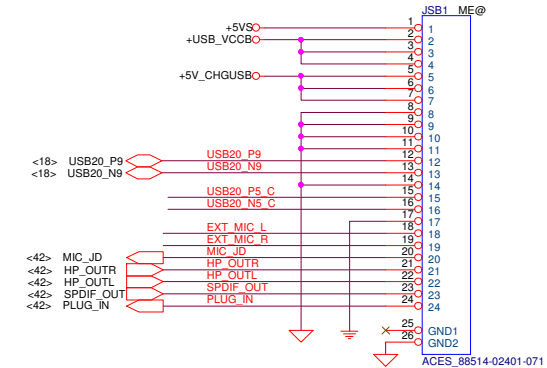
SEL Pin Decode

Pull Low
0R -1010_000
★ 10K-1010_000
12K-1010_000
15K-1010_000
18K-0110_000
22K-0110_000
27K-0110_000
33K-0110_000

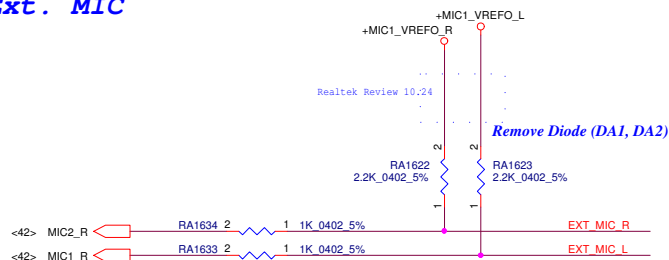
USB Power (USB20_P9)



AUDIO/B Conn.



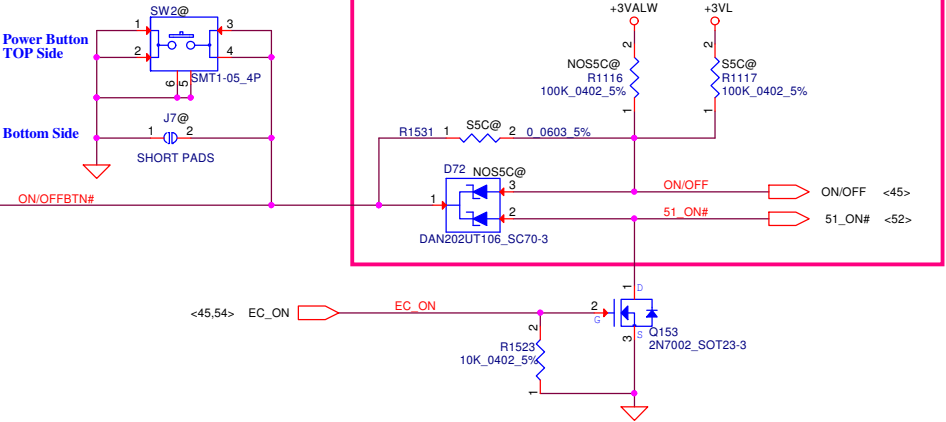
Ext. MIC



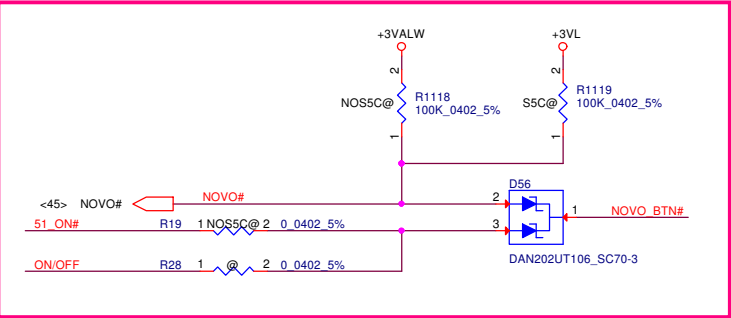
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	AUDIO/B, USB CHARGER
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ON/OFF switch

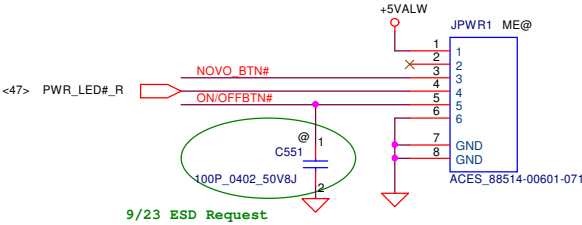
Support DC S5 Charge



Support DC S5 Charge



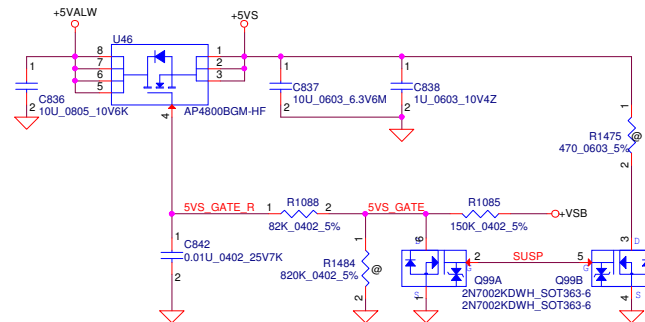
Power Button/B link
to Function/B Conn. 10pin



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

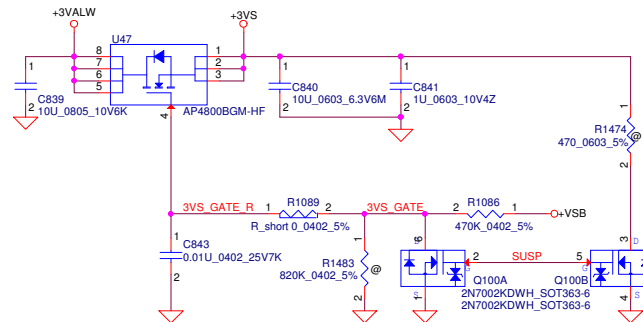
+5VALW to +5VS

AP4800BGM
VGS=1.0V, ID=9A, Rds=12m ohm
VGS=+2.5V

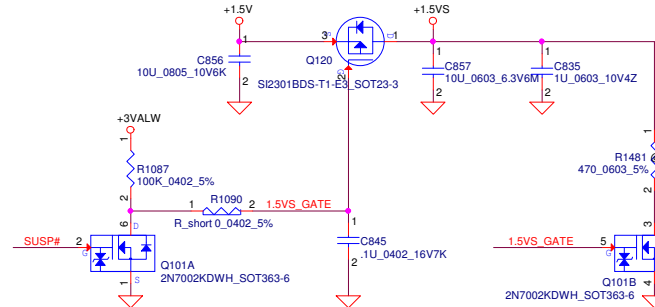
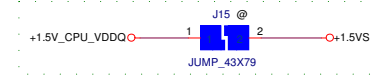


+3VALW to +3VS

AP4800BGM
VGS=1.0V, ID=9A, Rds=12m ohm
VGS=+2.5V

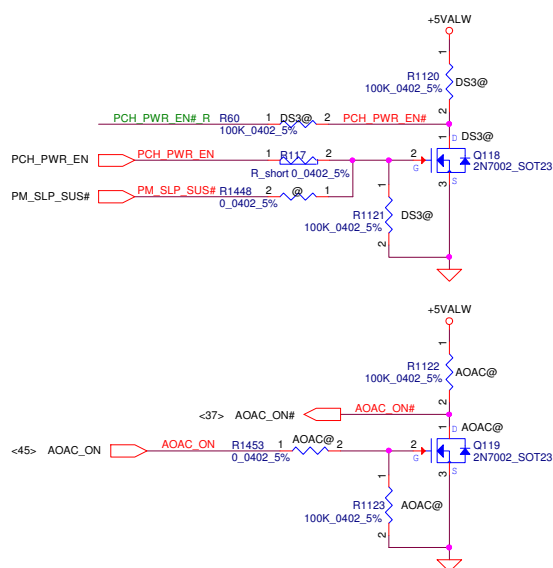
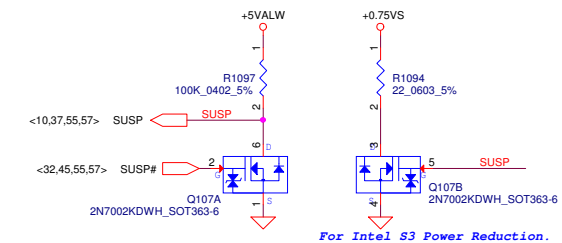
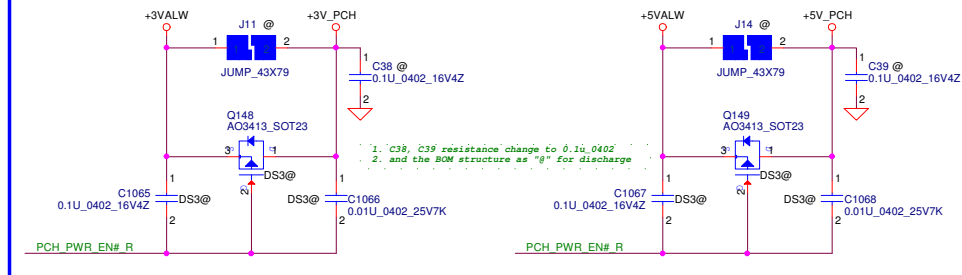


+1.5V to +1.5VS

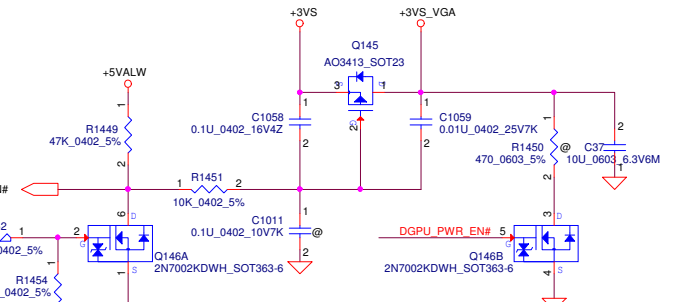
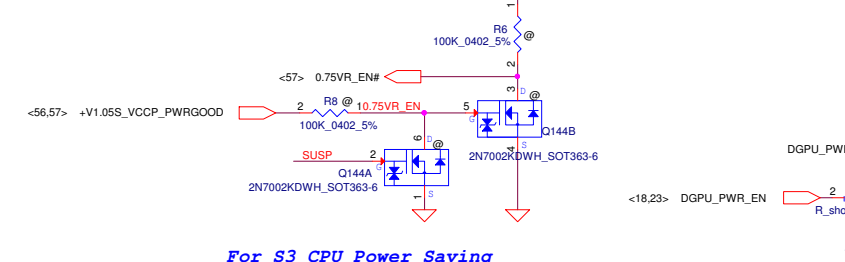


+3VALW to +3V_PCH

+5VALW to +5V_PCH

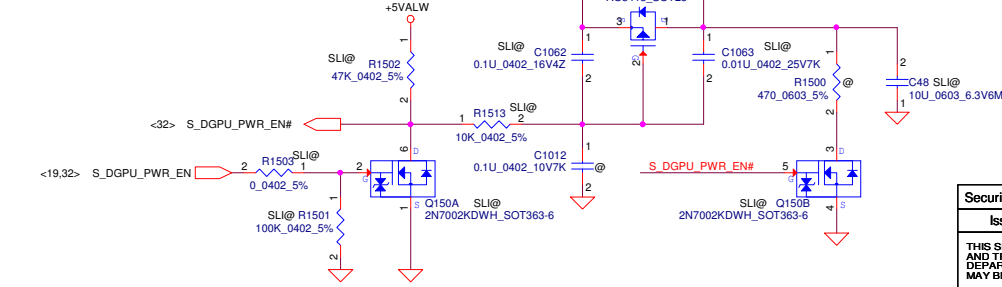


+3VS to +3VS_VGA

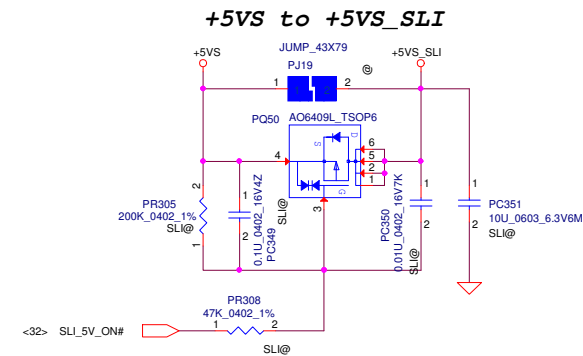
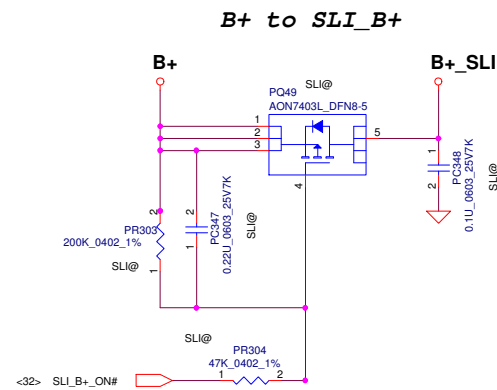
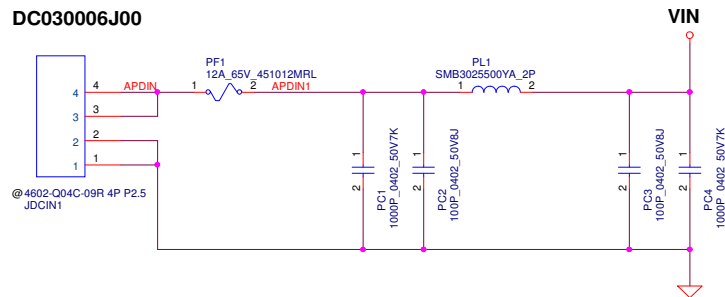


+3VS to +3VS_SLI

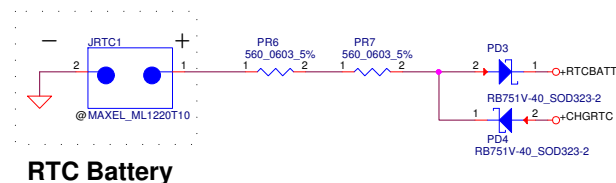
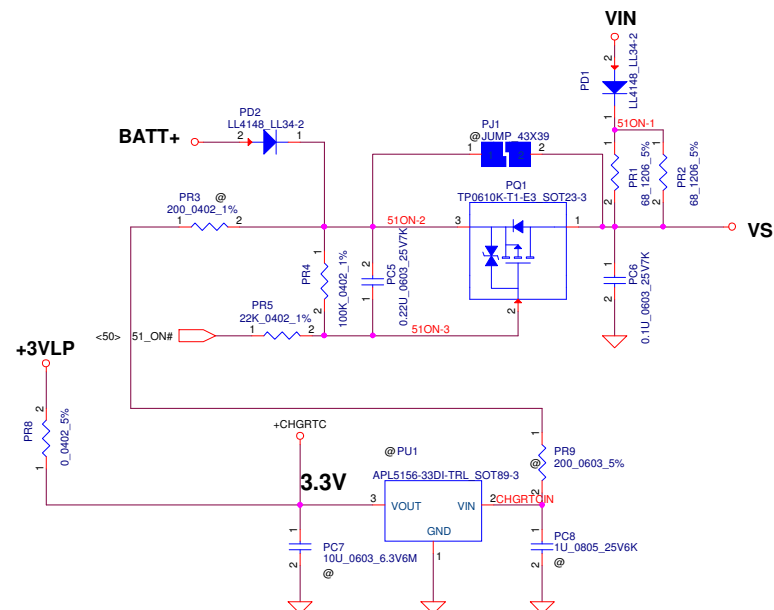
2012-0419 --> modify +3VS_SLI BOM structure to "SLI@"




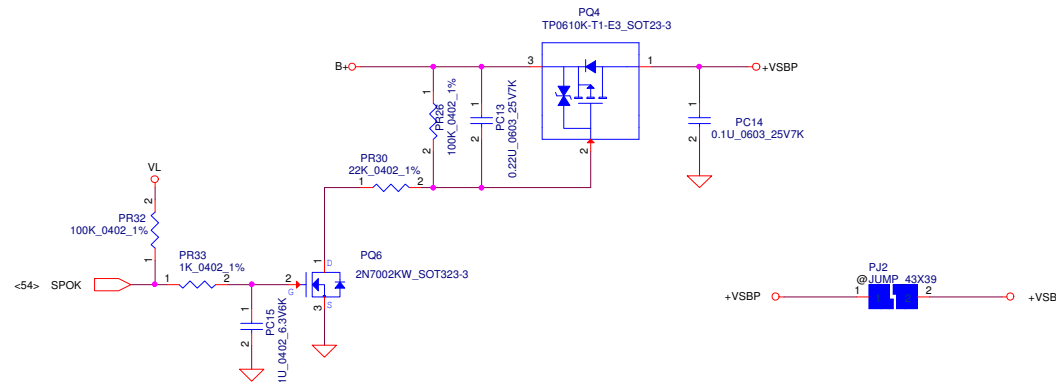
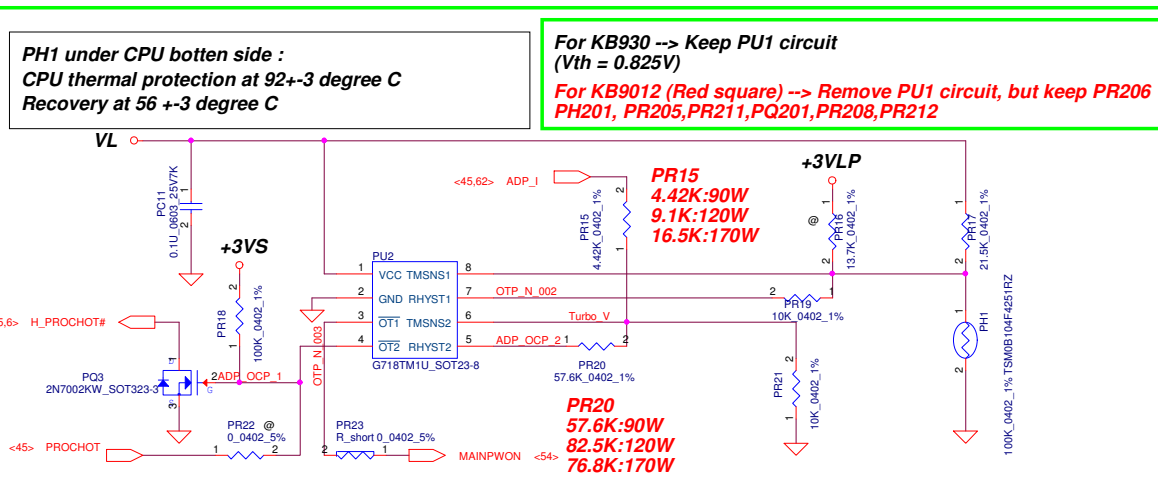
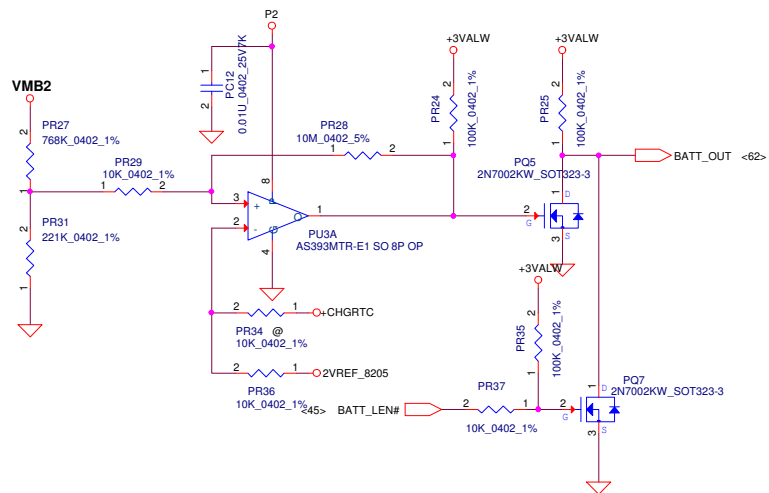
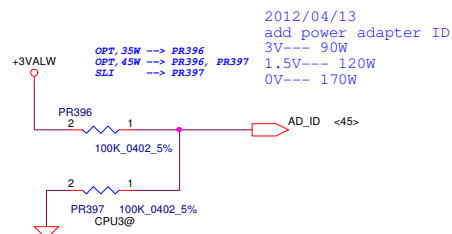
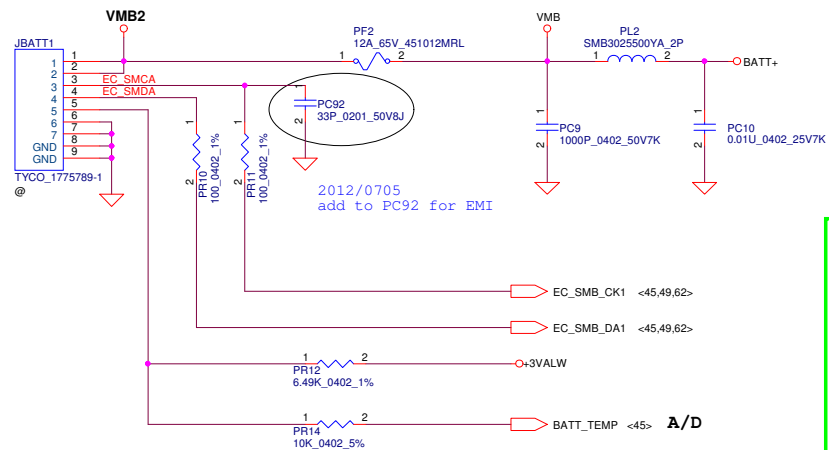
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	DC INTERFACE	
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2012/04/13
add SLI Hot-plug Load-SW solution

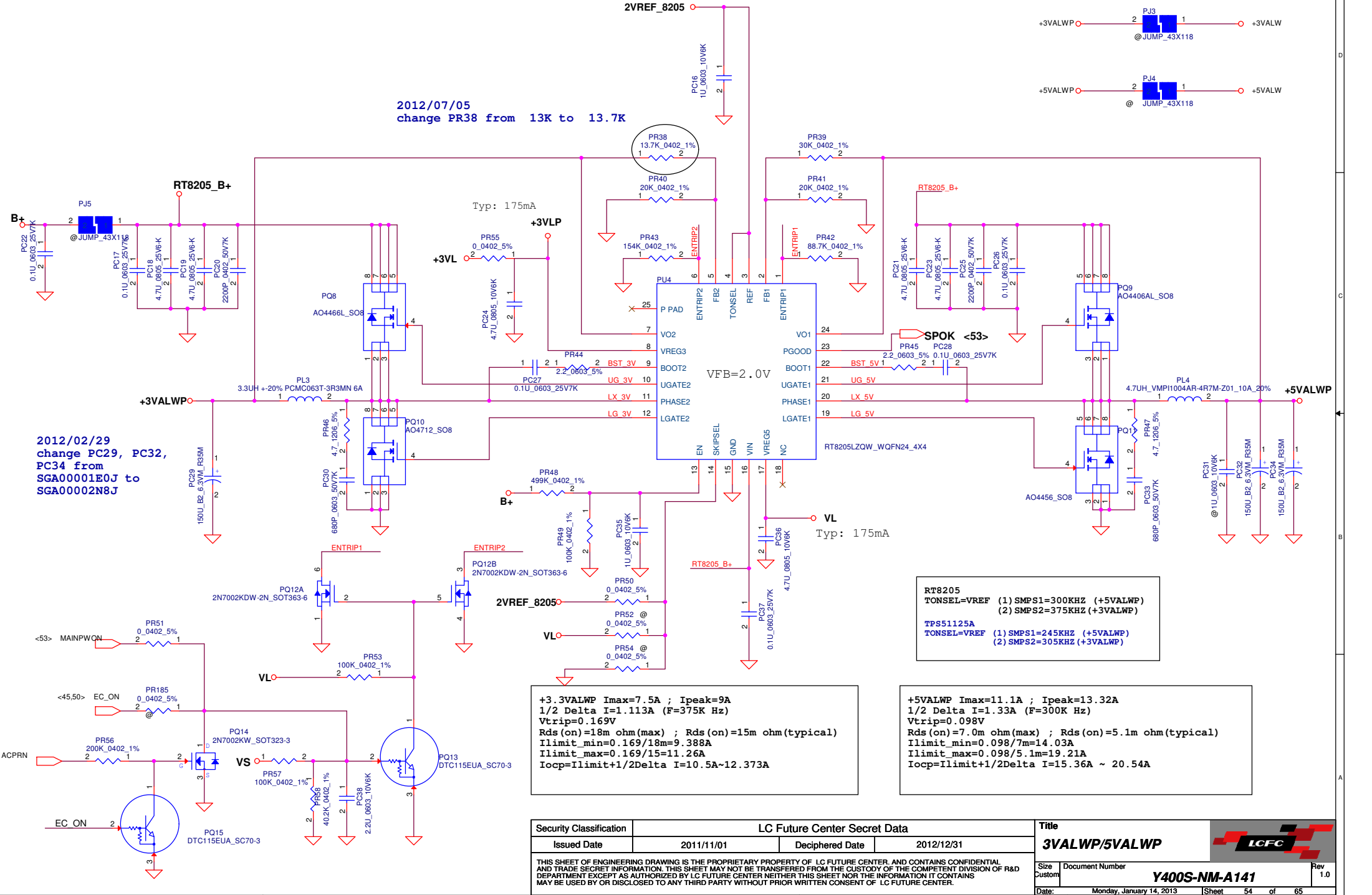



Security Classification		LC Future Center Secret Data		Title		
Issued Date	2011/1/1/01	Deciphered Date	2012/12/31	VIN DETECTOR		
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				Date:	Monday, January 14, 2013	Sheet 52 of 65 Rev 1.0

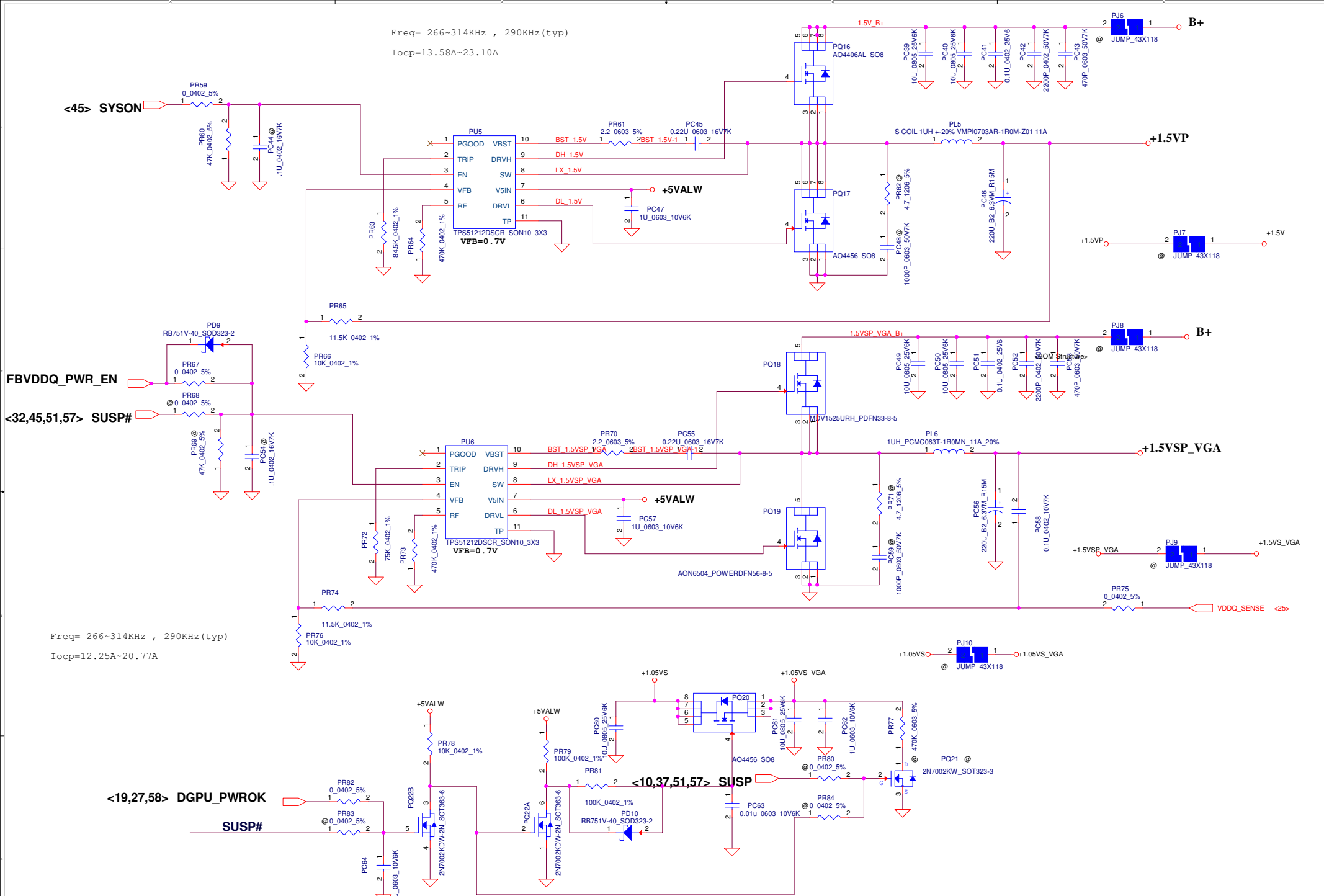


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Date: Monday, January 14, 2013				Sheet 53 of 65

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

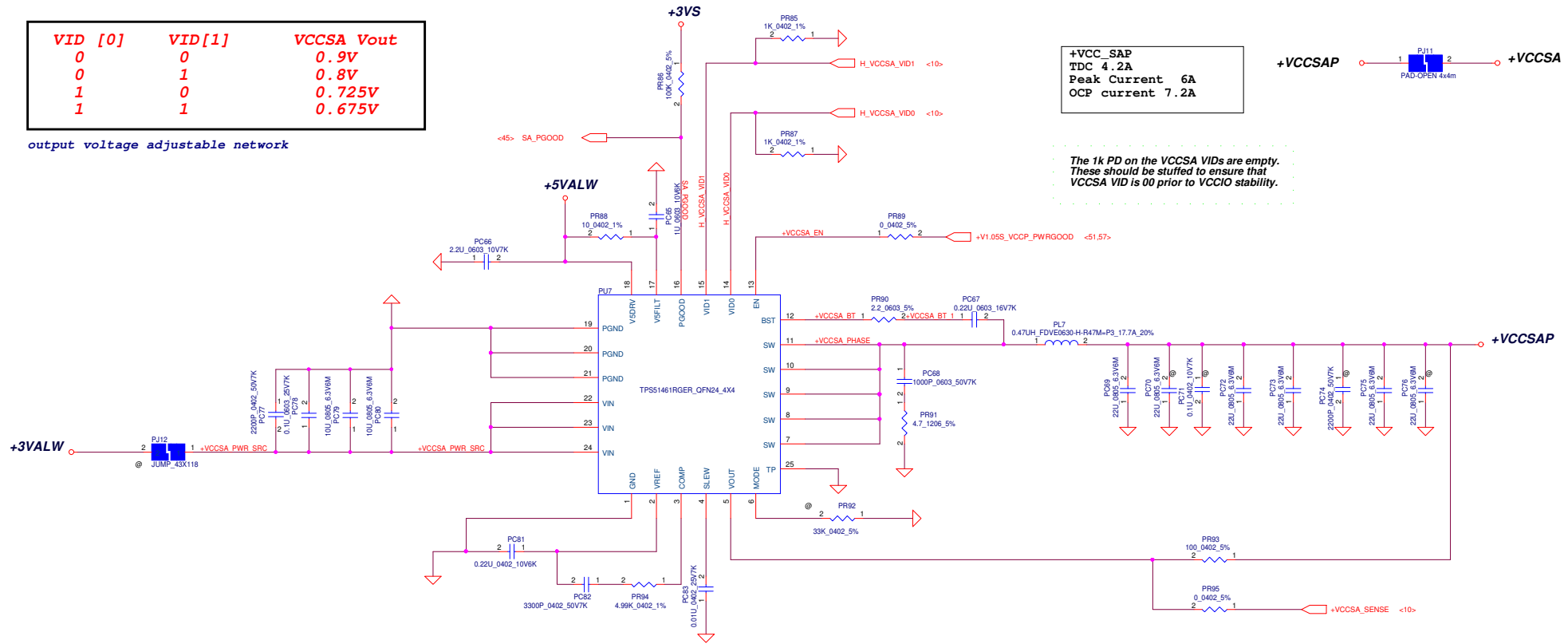


Security Classification		LC Future Center Secret Data				Title			
Issued Date		2011/11/01		Deciphered Date		2012/12/31			
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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

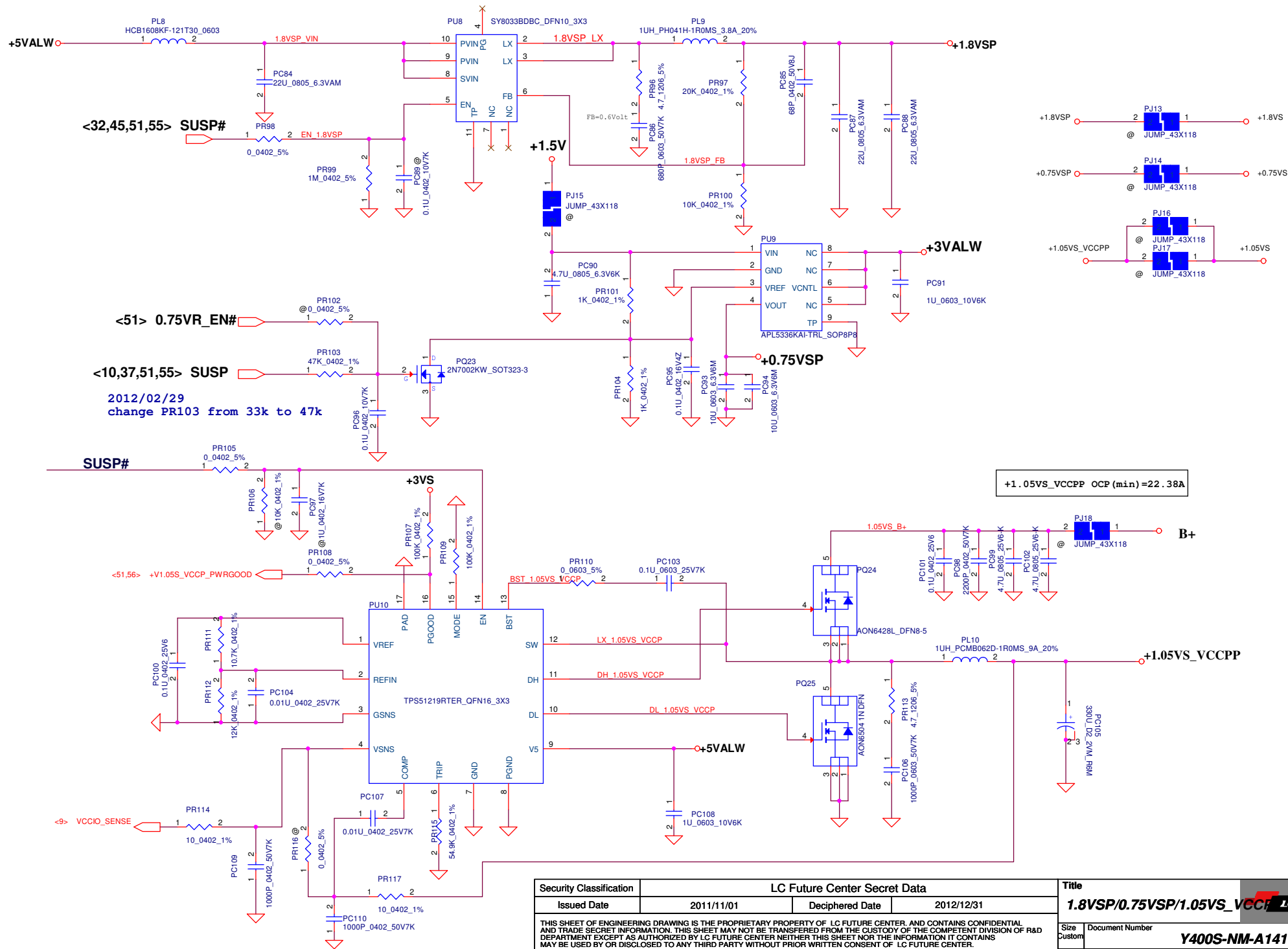
output voltage adjustable network



+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

+VCCSAP

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

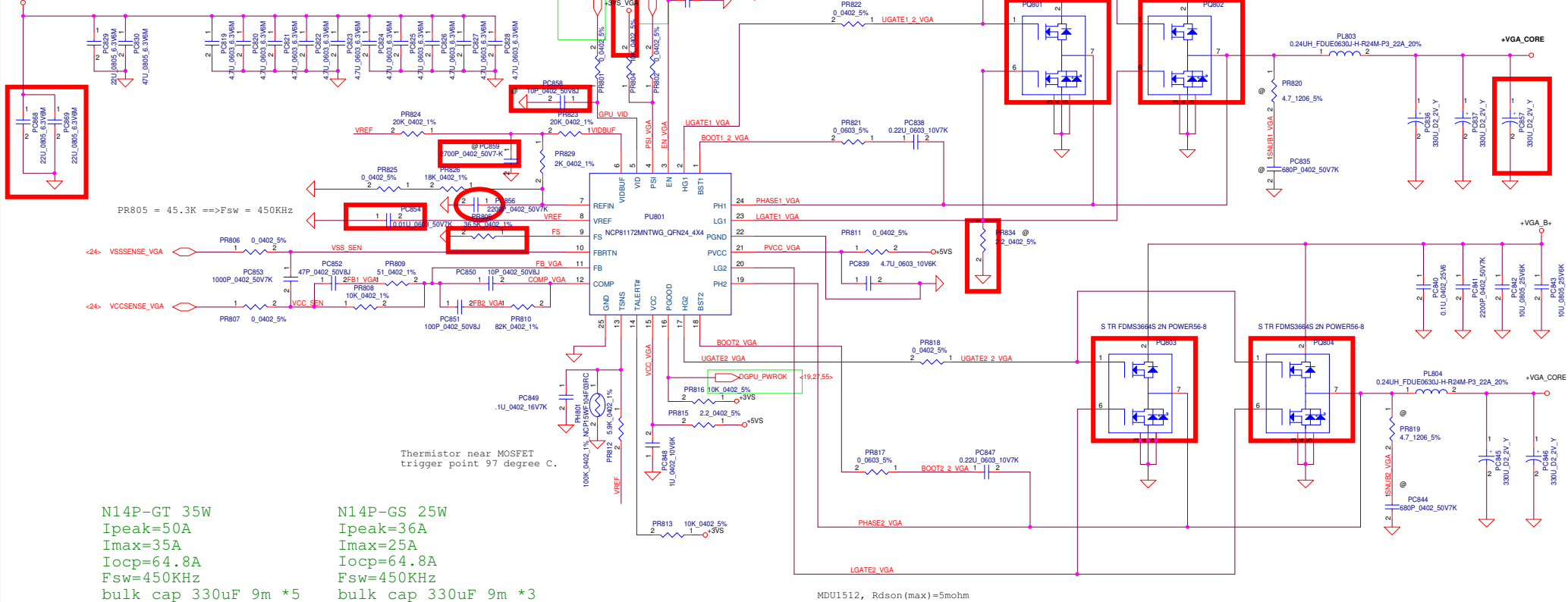


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	1.8VSP/0.75VSP/1.05VS_VCCF ICFC	
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				Rev	1.0

+VGA_CORE Under VGA Core GB4-128 package

+VGA_CORE

Near VGA Core

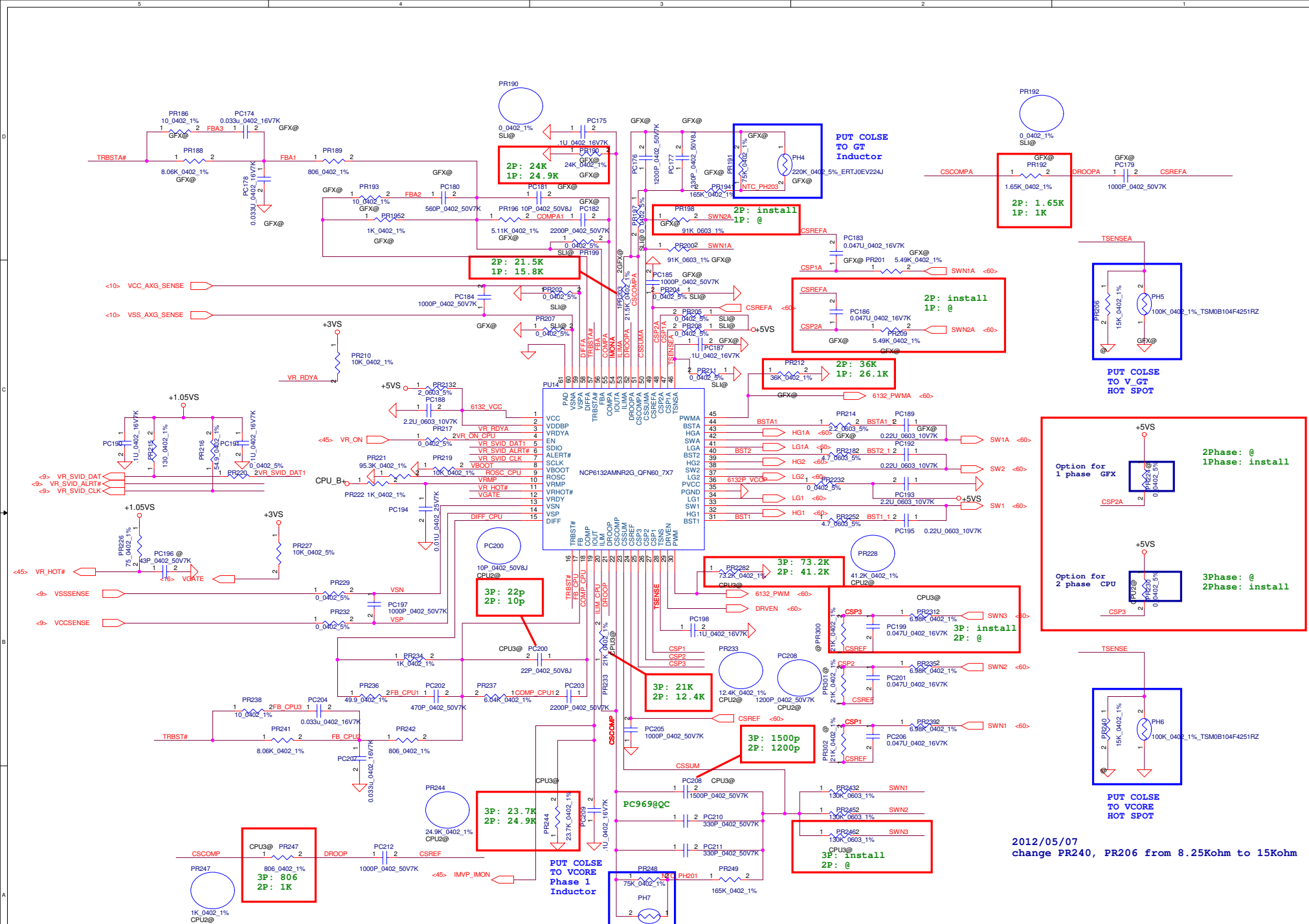


N14P-GT 35W
Ipeak=50A
Imax=35A
Iocp=64.8A
Fsw=450KHz
bulk cap 330uF 9m *5

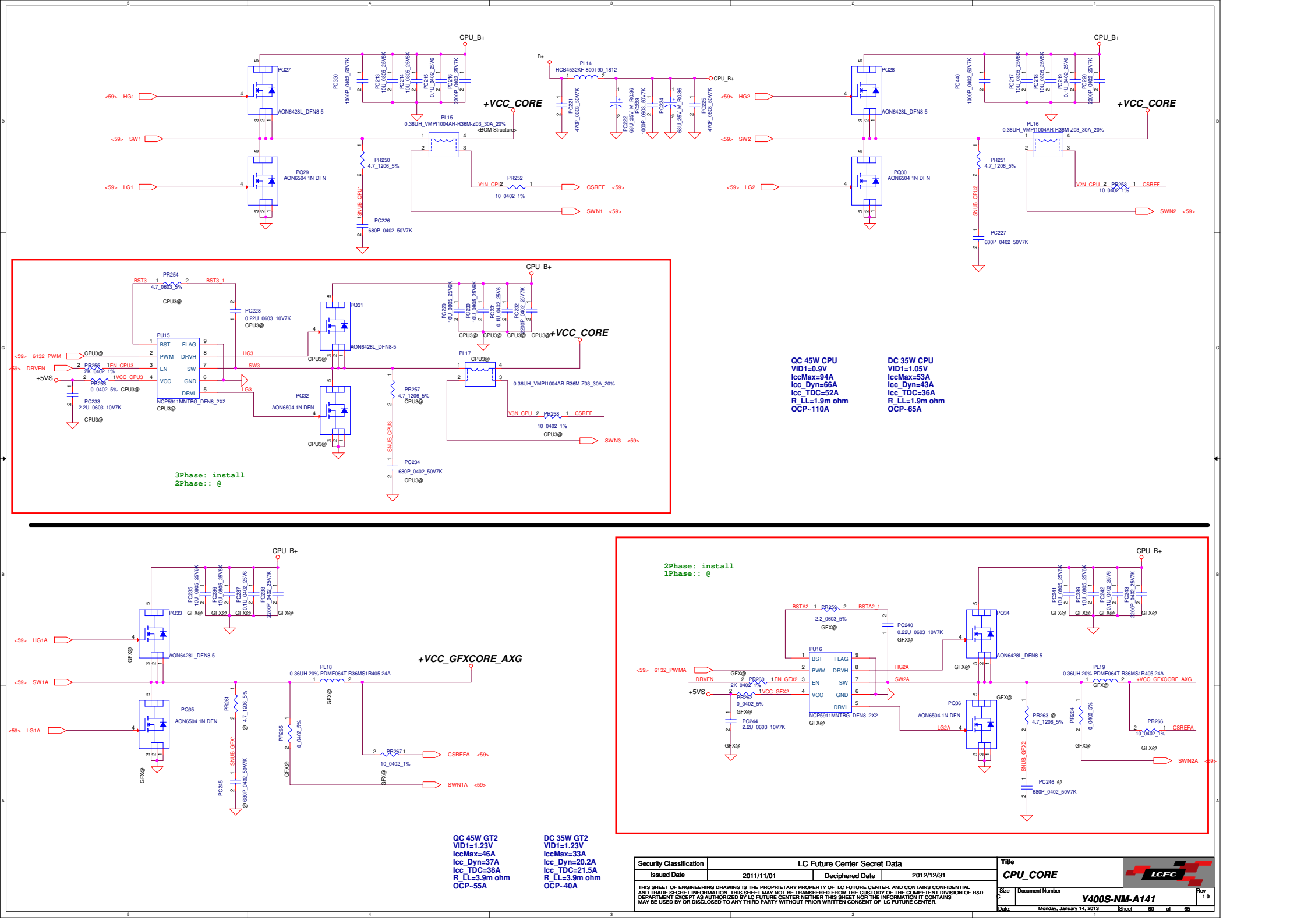
N14P-GS 25W
Ipeak=36A
Imax=25A
Iocp=64.8A
Fsw=450KHz
bulk cap 330uF 9m *3

Thermistor near MOSFET
trigger point 97 degree C.

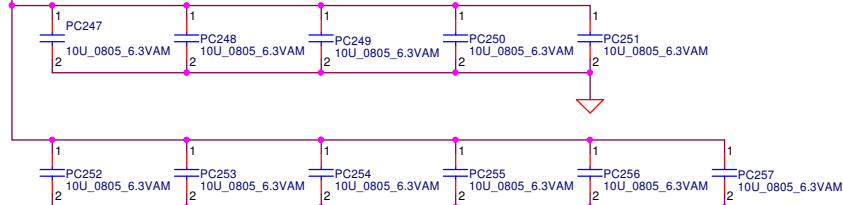
MDU1512, Rds(on)=5mohm



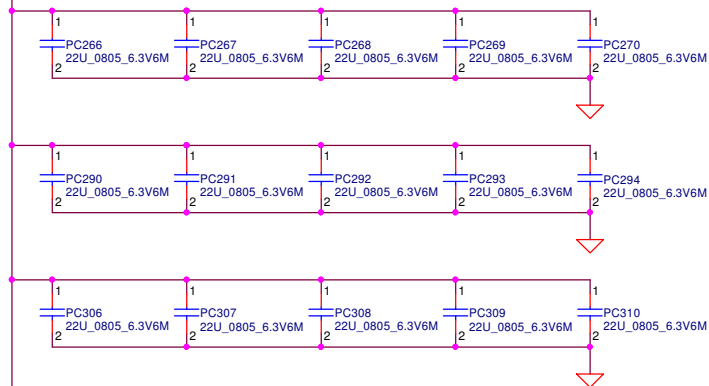
2012/05/07
change PR240, PR206 from 8.25Kohm to 15Kohm



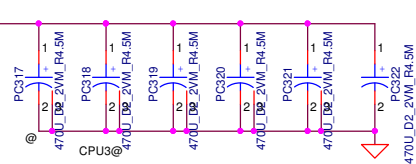
+VCC_CORE



+VCC_CORE



+VCC_CORE



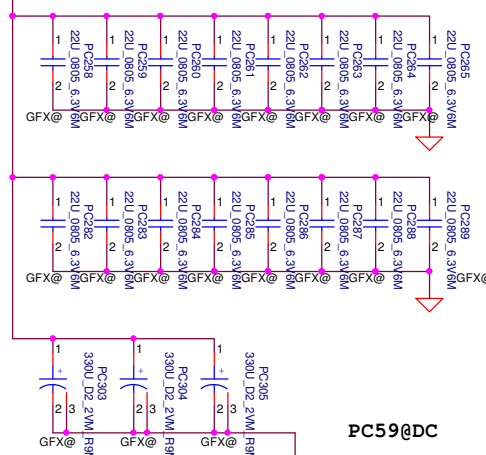
DC: PC73, PC74, PC75, PC76, PC77, PC78 (330uF/9m)
QC: PC76, PC78 (470uF/4.5m), PC73, PC74, PC75 (330uF/9m)

PC8, PC21, PC22, PC63

+CPU_CORE

+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG



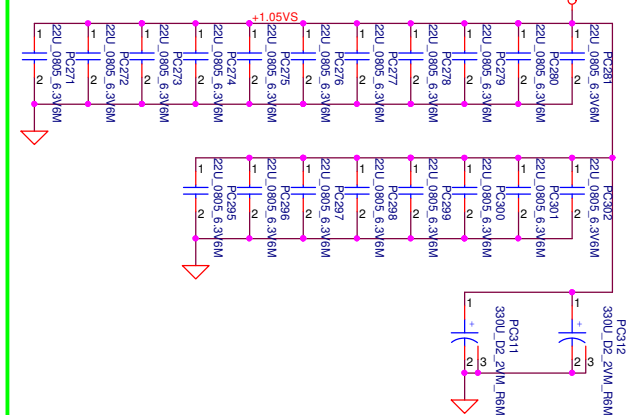
PC38, PC39, PC40, PC41

PC38, PC39, PC40, PC41

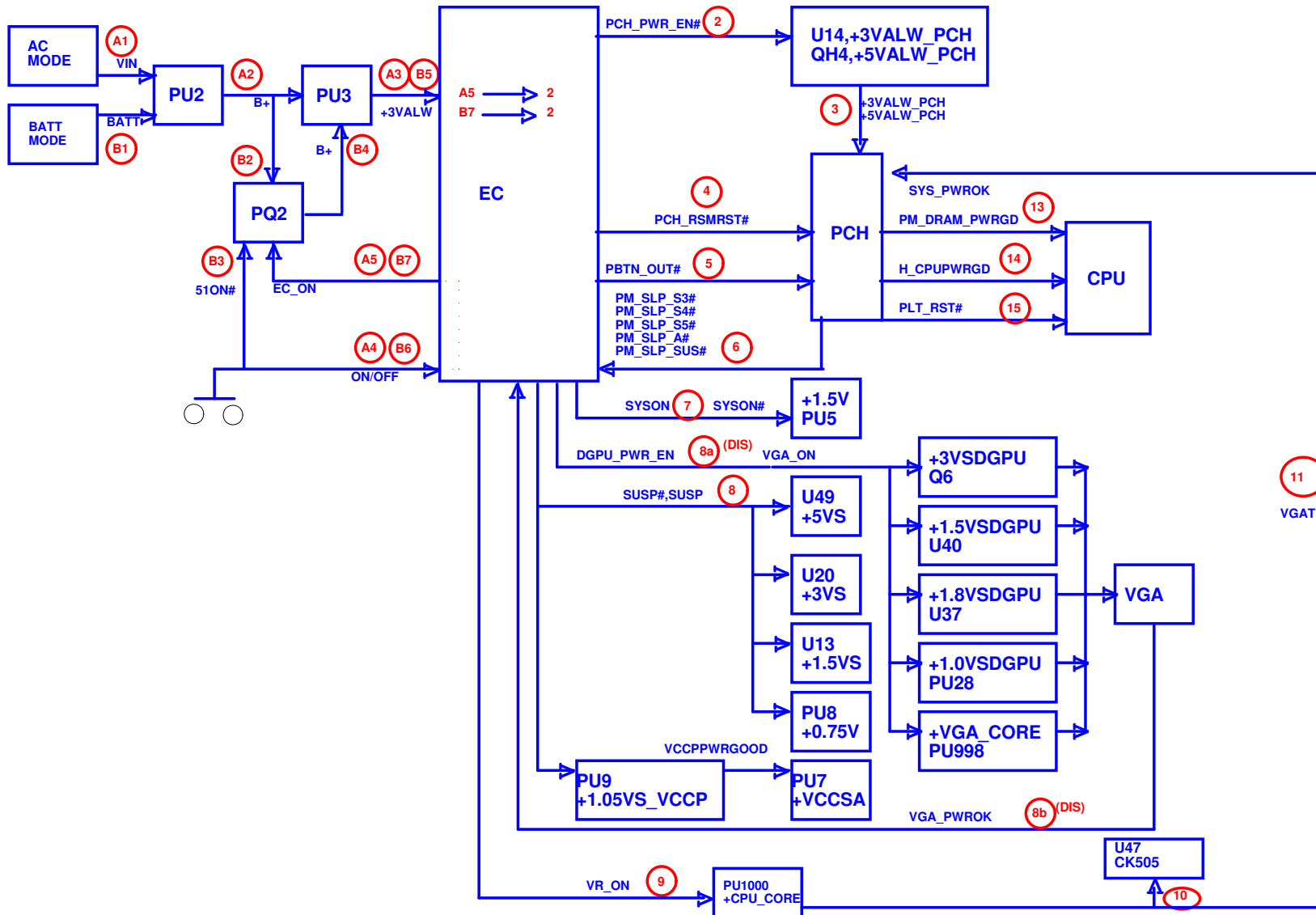
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05VS



PC32, PC49, PC54, PC55, PC56



Item	Reason for change	PG#	Modify List	Date	Phase
1	For NV suggest	58	Add (reserve parts) PC859		
2	For TI suggest	58	Add (reserve parts) PR834		
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

QIWY5 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1		P23	Change DGPU_PWR_EN to PLT_RST_VGA#	EVT TO DVT
2		P23	Add CV148	For GC6 function
3				For GC6 function
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				